

202120-0005/001

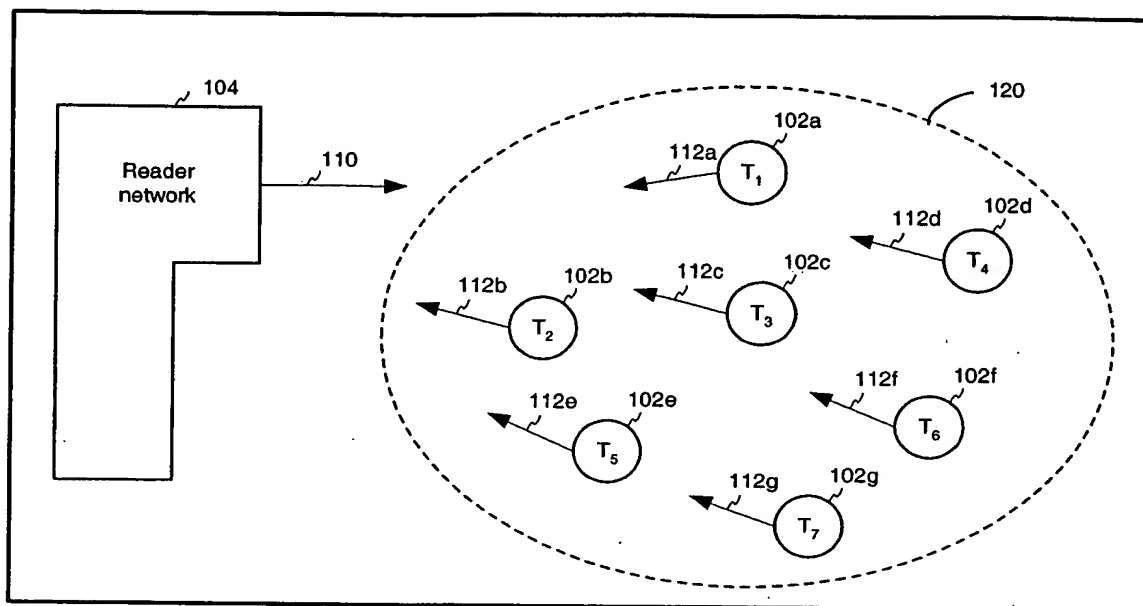


FIG. 1

# Reader Network / Site

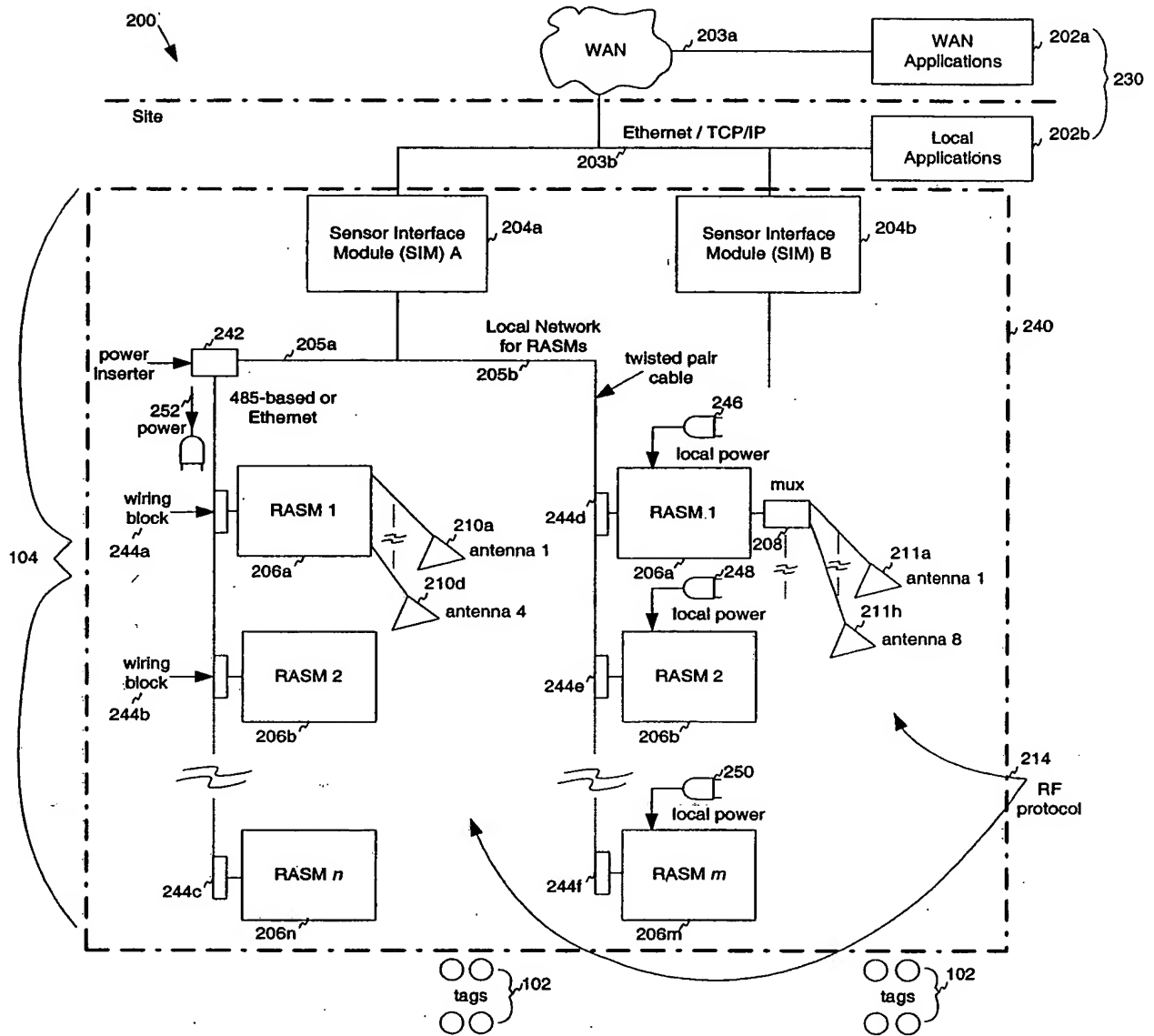


FIG. 2

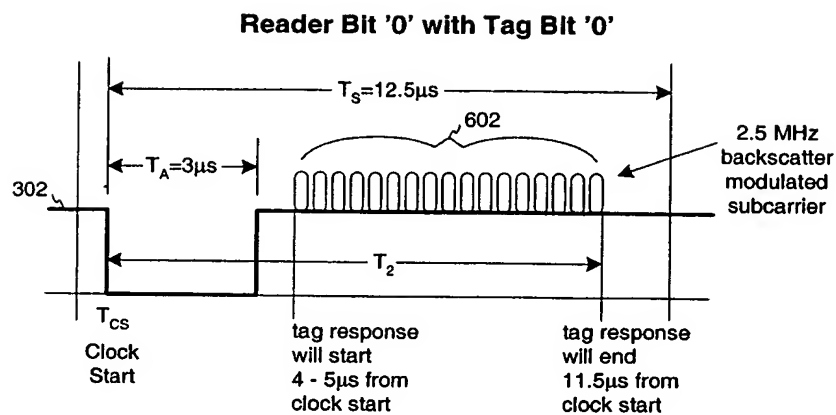
Timing diagram for Reader Data '0'. The signal  $S$  transitions from  $S_{\text{high}}$  to  $S_{\text{low}}$  at time  $T_{\text{CS}}$ . The signal remains at  $S_{\text{low}}$  for a duration  $T_A = 3\mu\text{s}$  before returning to  $S_{\text{high}}$ . The total time interval shown is  $T_s = 12.5\mu\text{s}$ . The signal level  $S_{\text{high}}$  is labeled as 302.

Timing diagram for Reader Data '1'. The signal  $S$  is high for  $T_S = 12.5 \mu s$  and low for  $T_B = 6 \mu s$ . The total period is  $T_{CS}$ . The signal level is labeled 402.

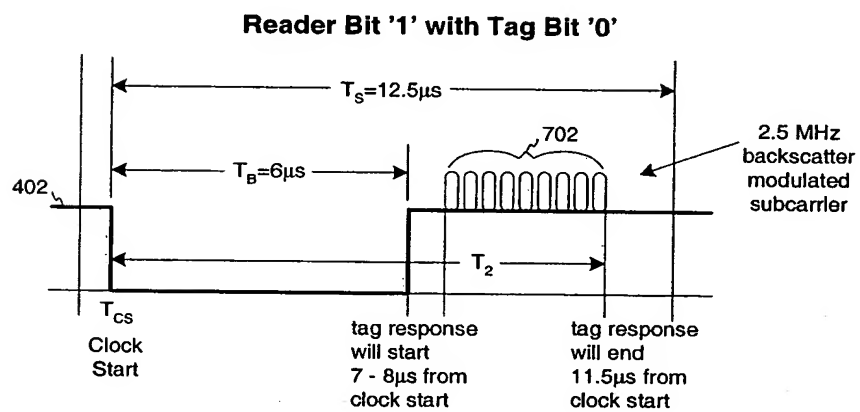
Timing diagram for Reader Data 'null'. The vertical axis represents signal level  $S$ , with  $S_{high}$  and  $S_{low}$  levels indicated. The horizontal axis represents time. The signal  $S$  is high for a duration  $T_s = 12.5\mu s$  and then transitions to low for a duration  $T_c = 9.5\mu s$ . The total duration of the signal is  $22\mu s$ . The signal is labeled '502'.

0201-20b.vsd/3

10074000 000E/001



**FIG. 6**



**FIG. 7**

Reader Bit '0' with Tag Bit '1'

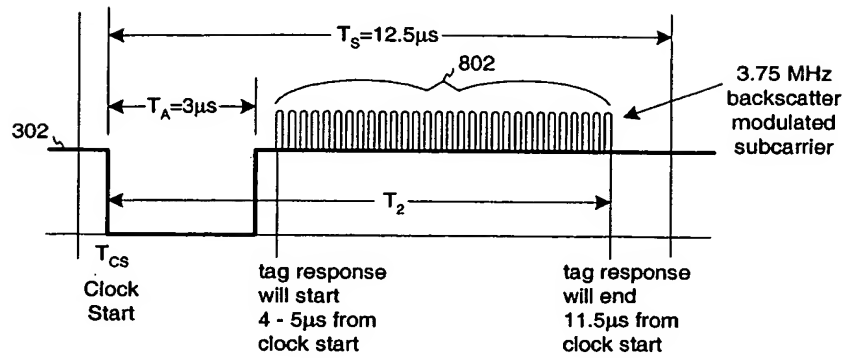


FIG. 8

Reader Bit '1' with Tag Bit '1'

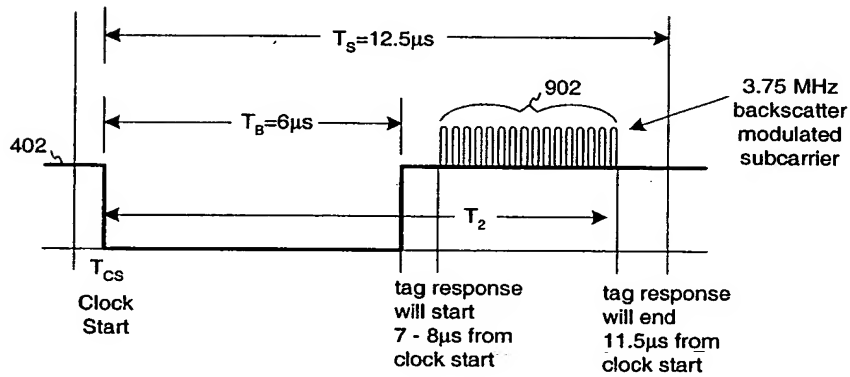


FIG. 9

2001-20b.vsd

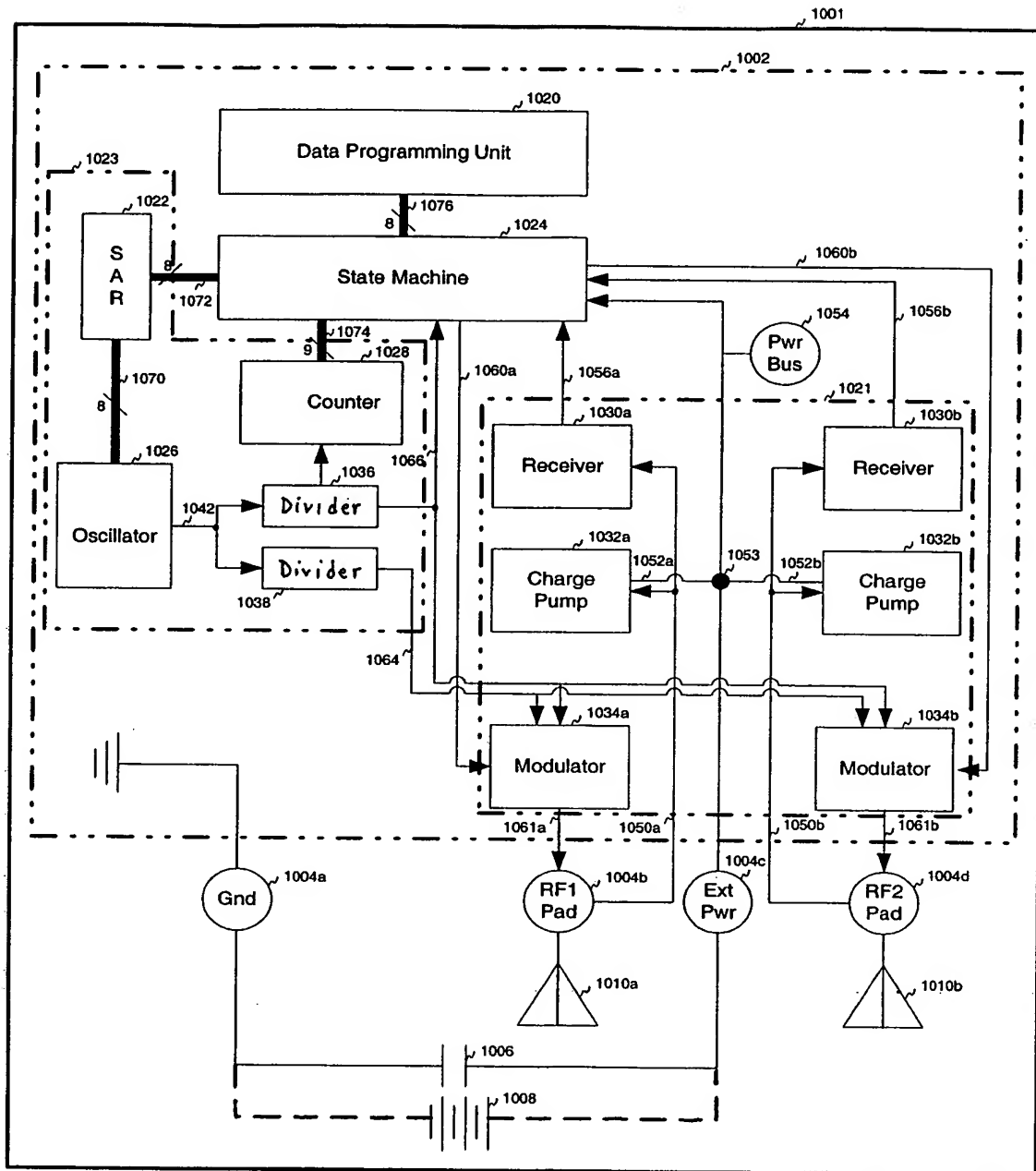


FIG. 10

0201-20b.vsd/7

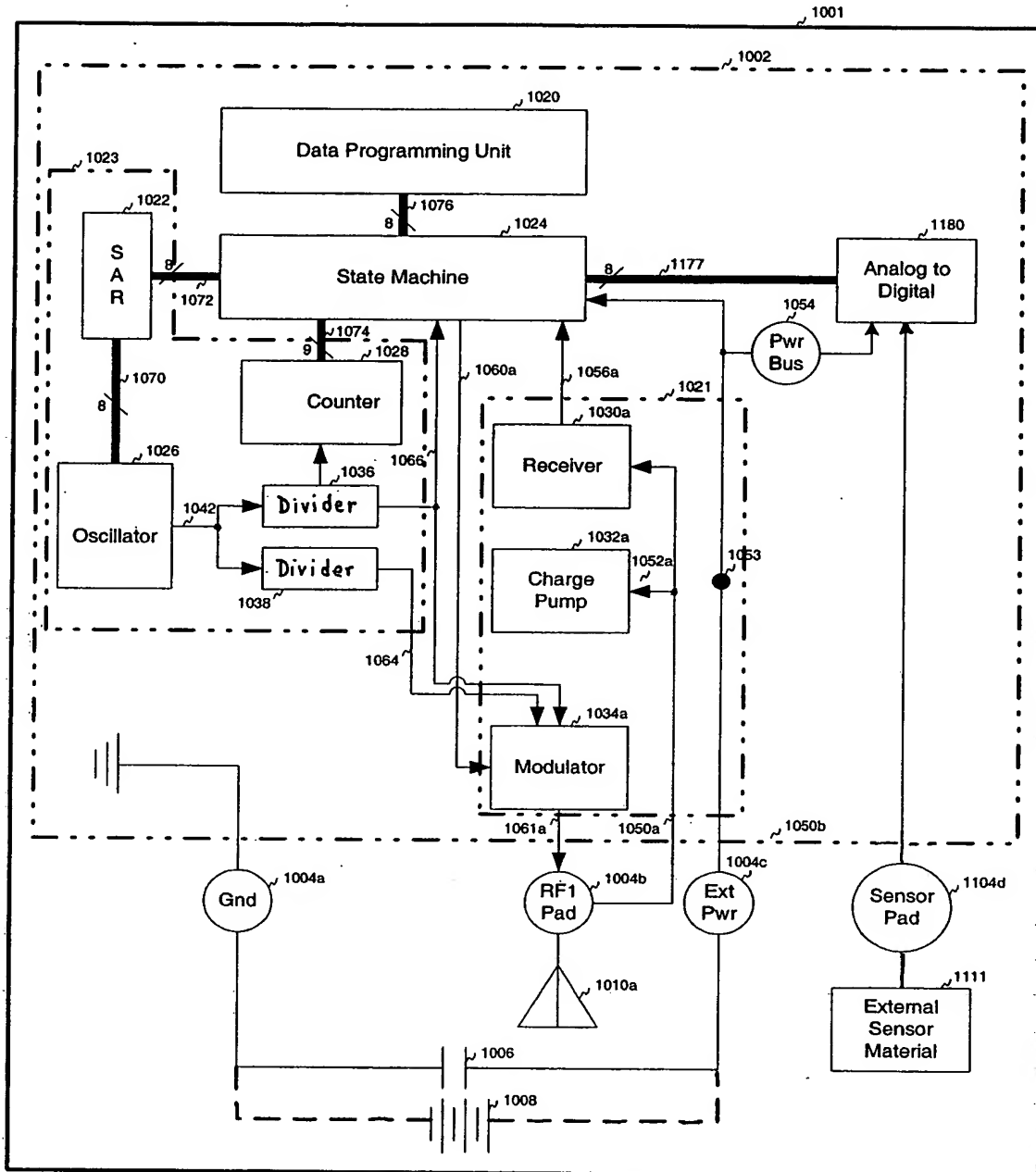


FIG. 11

20073000-001200

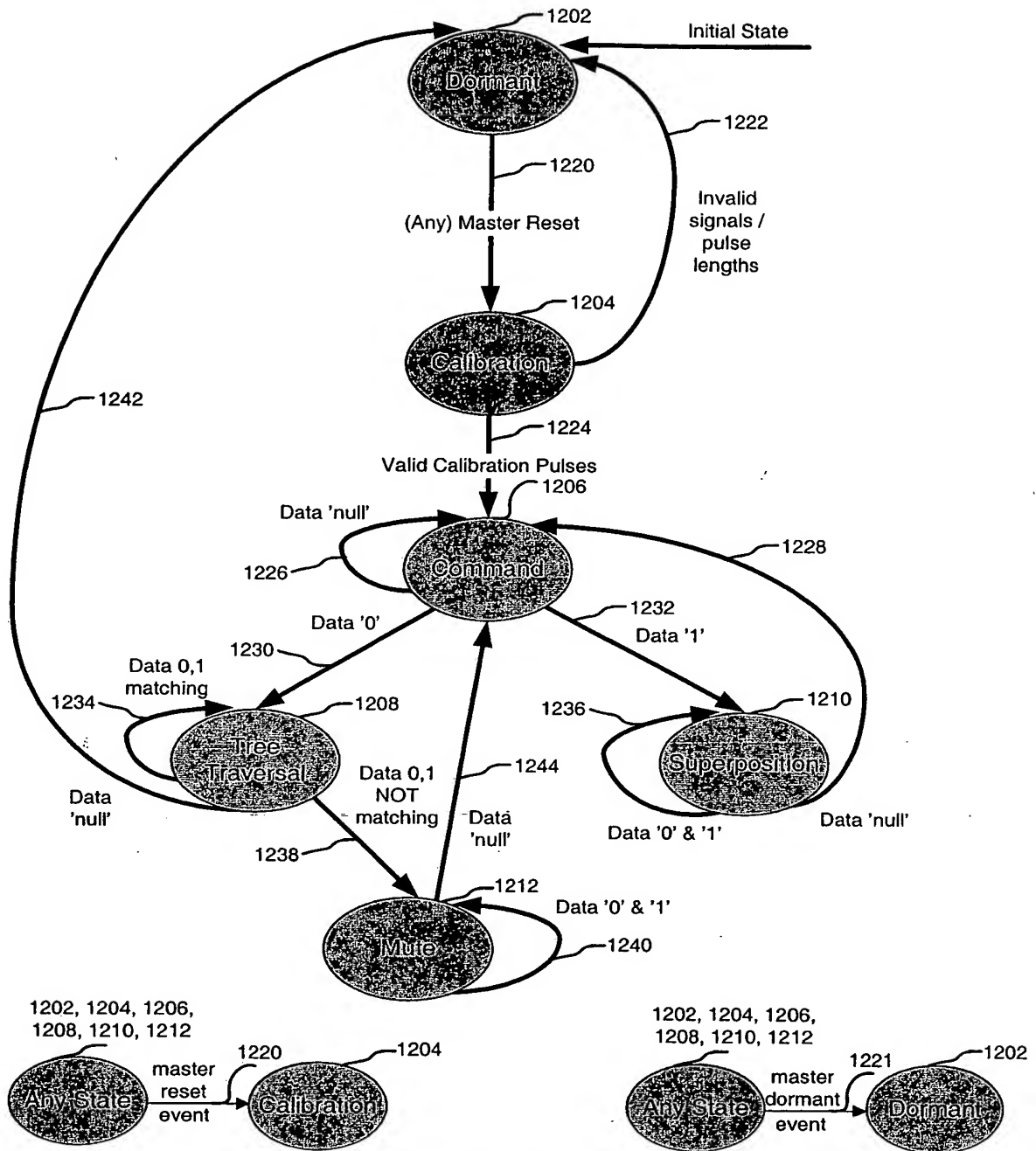


FIG. 12A



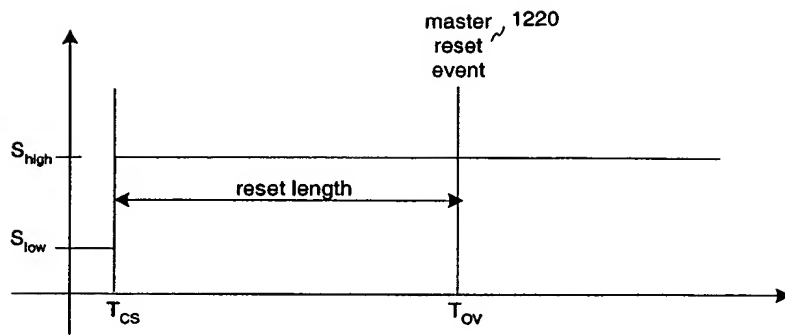


FIG. 12B

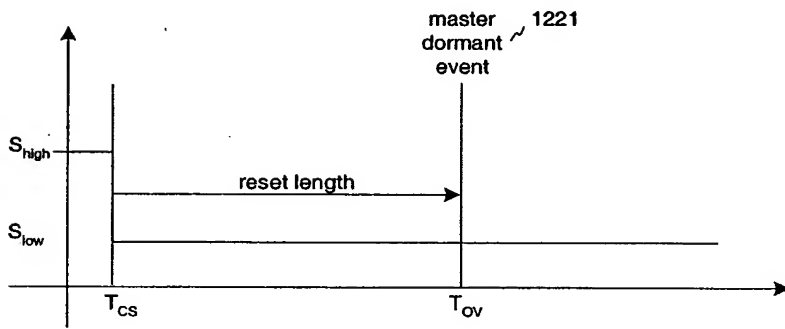


FIG. 12C

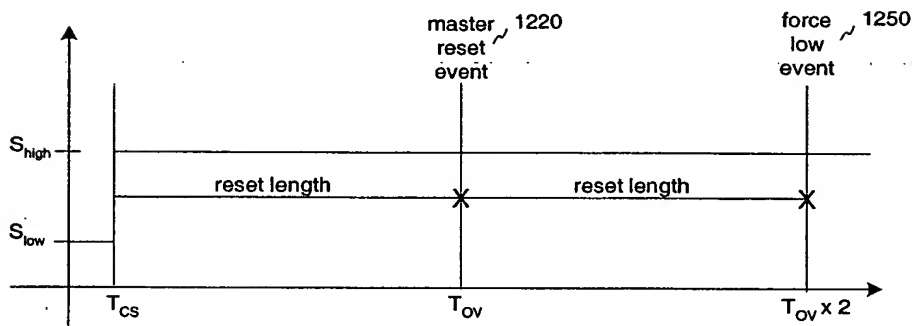


FIG. 12D

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# Binary Traversal Flowchart from a Tag Perspective

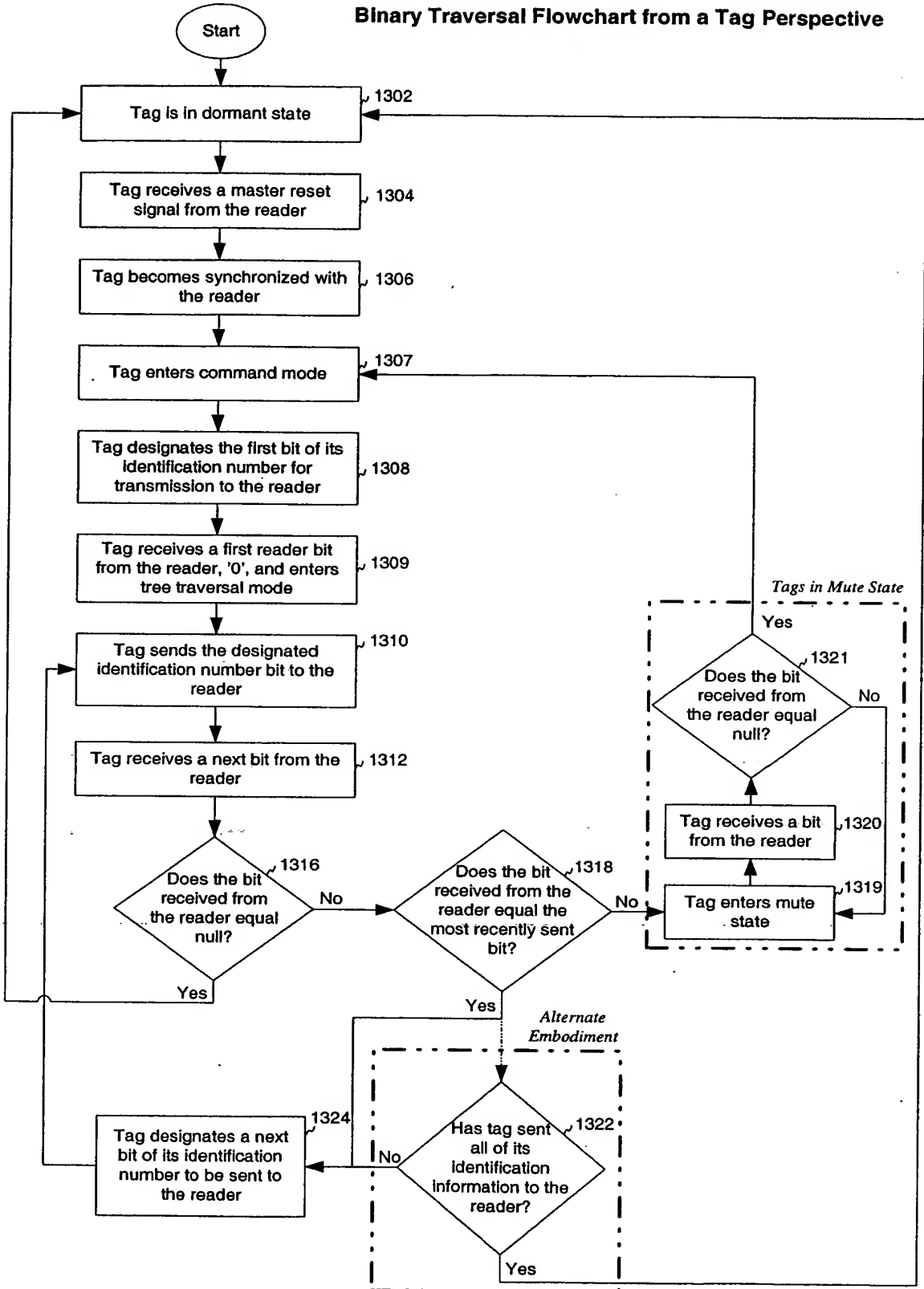


FIG.13

# Read Specific Tag, Reader Perspective

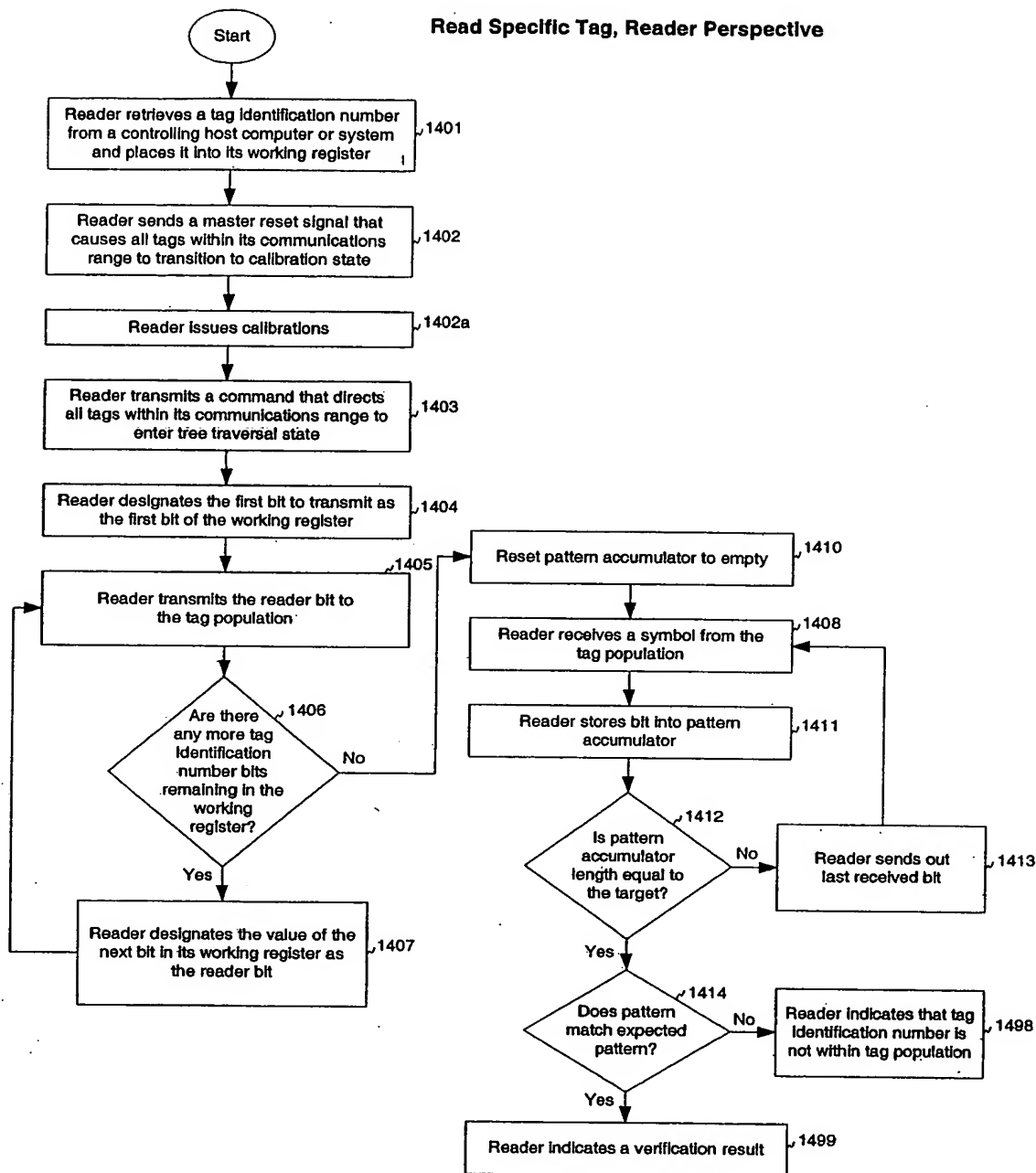
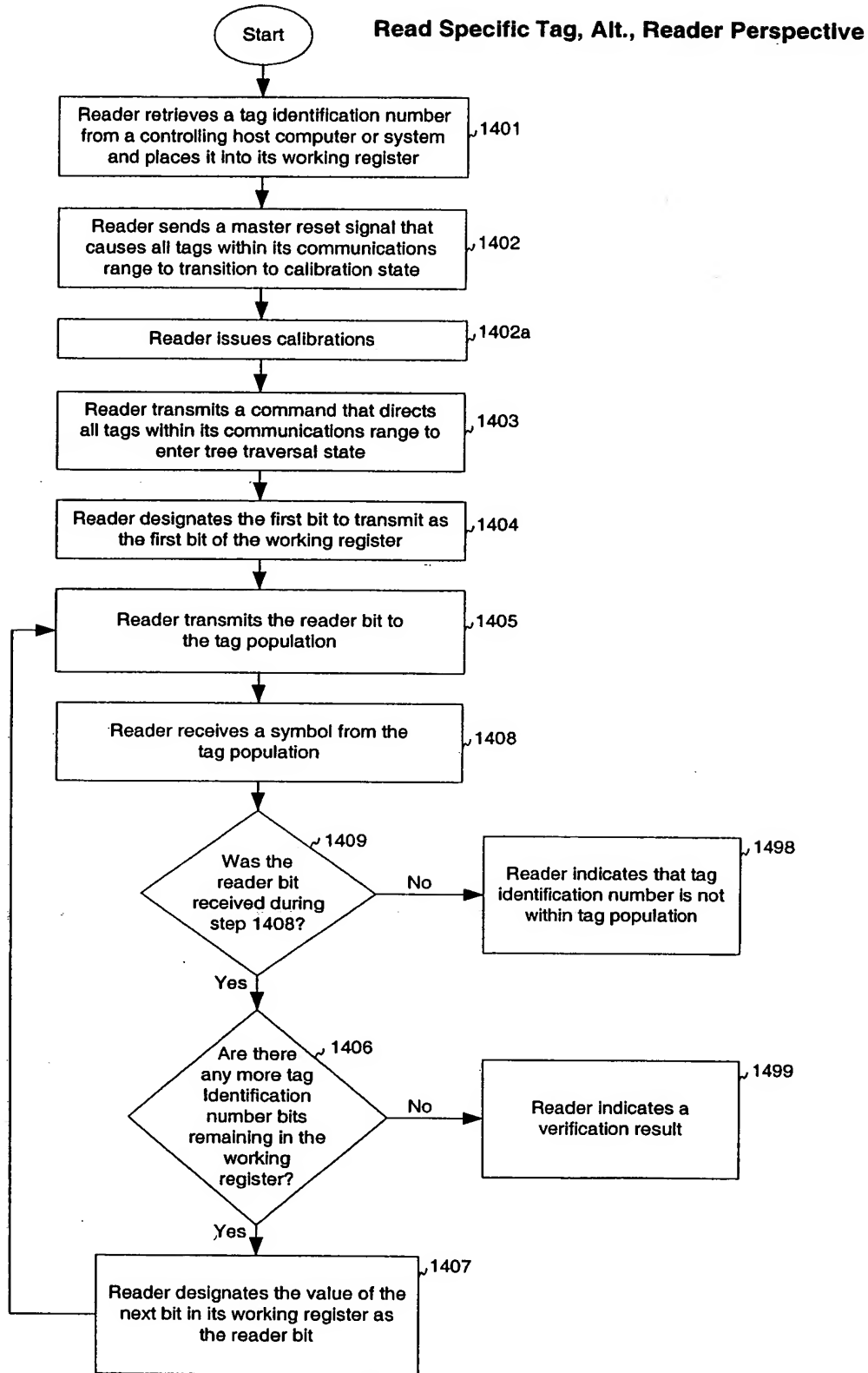
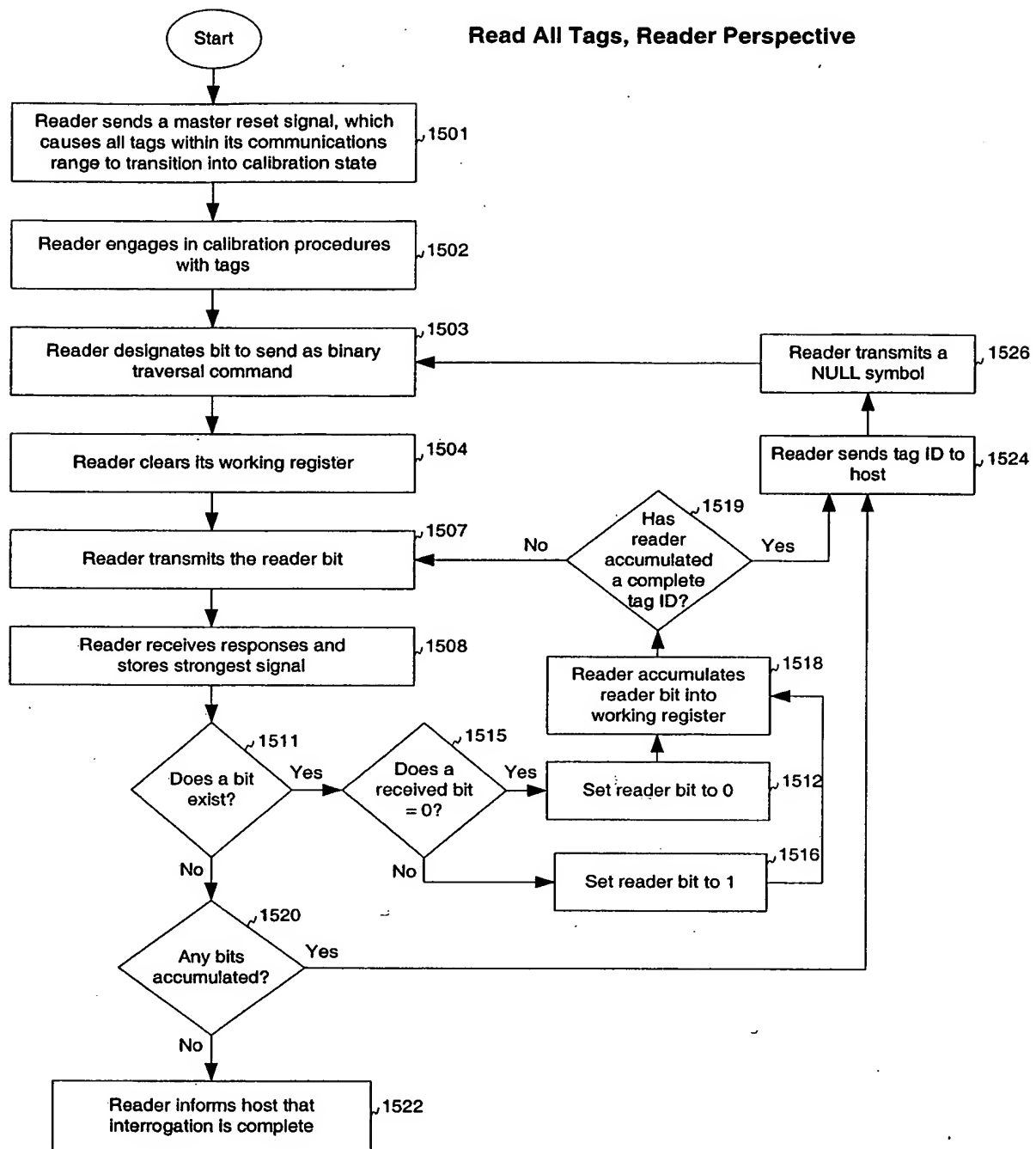


FIG. 14A

2021-20b.vsd/12

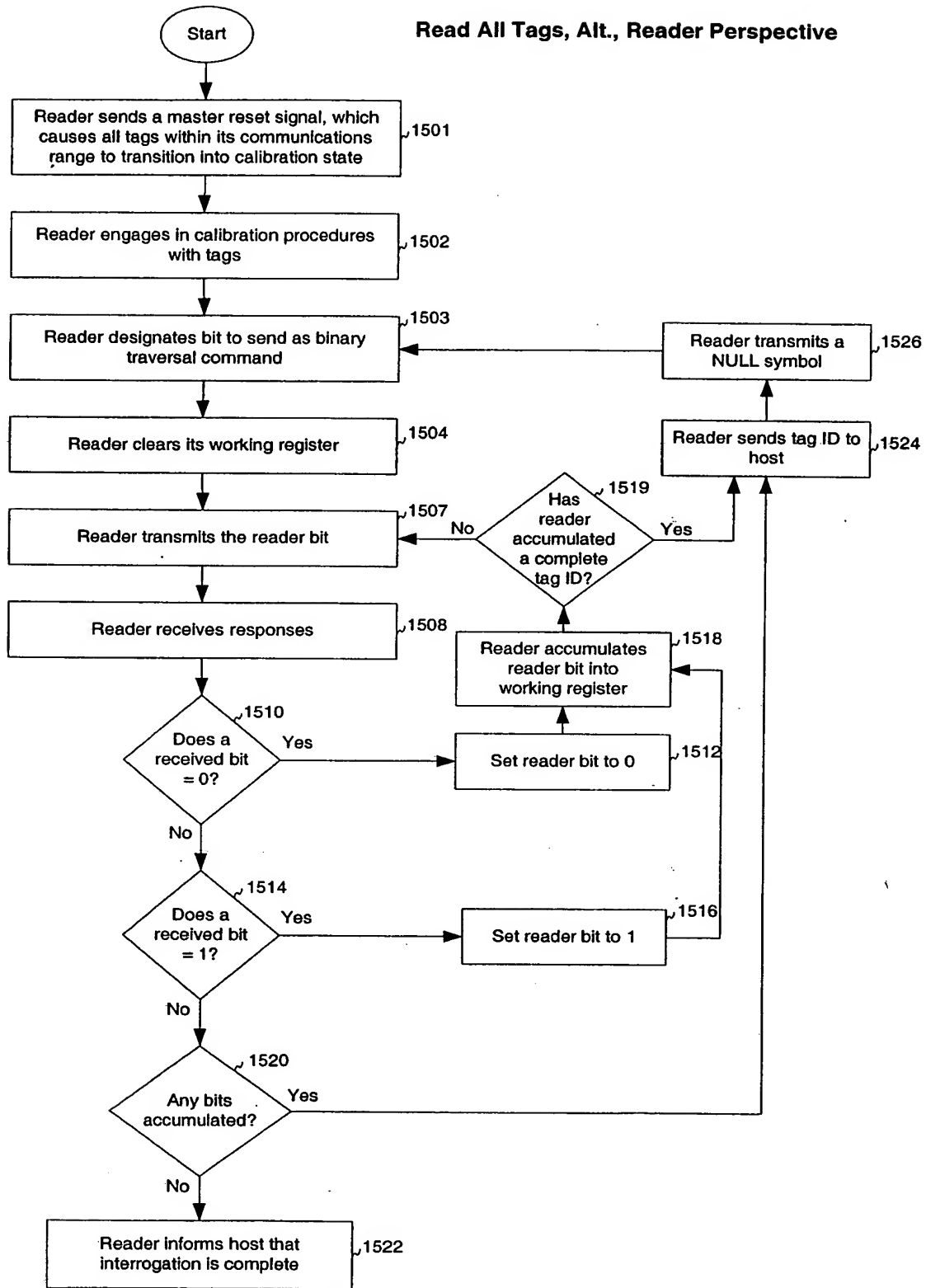


**FIG. 14B**



**FIG. 15A :**

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**FIG. 15B**

# Binary Traversal Paths and Tree for a 3-bit Tag Population

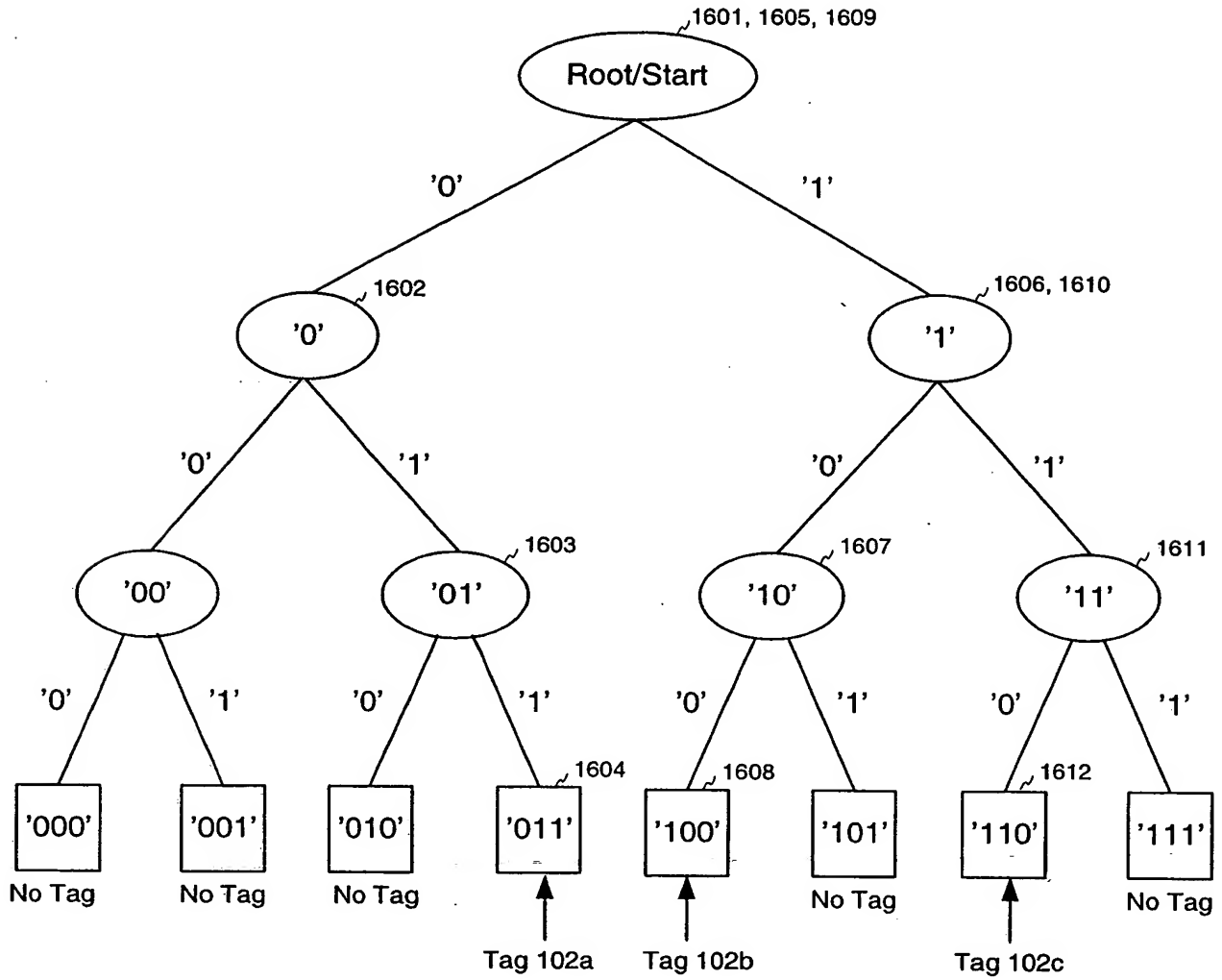


FIG. 16

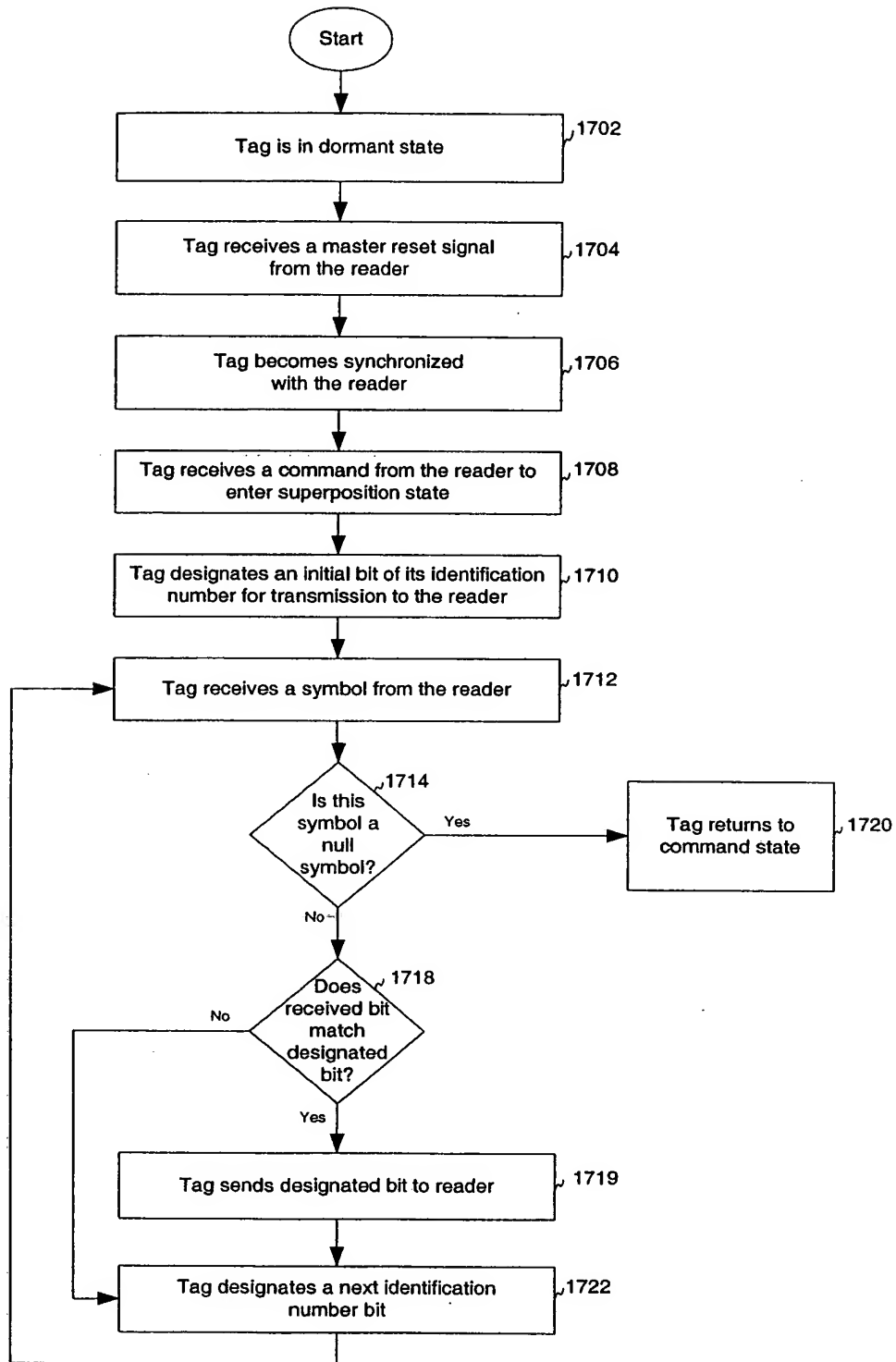


FIG. 17A



2021-20b.vsd/17

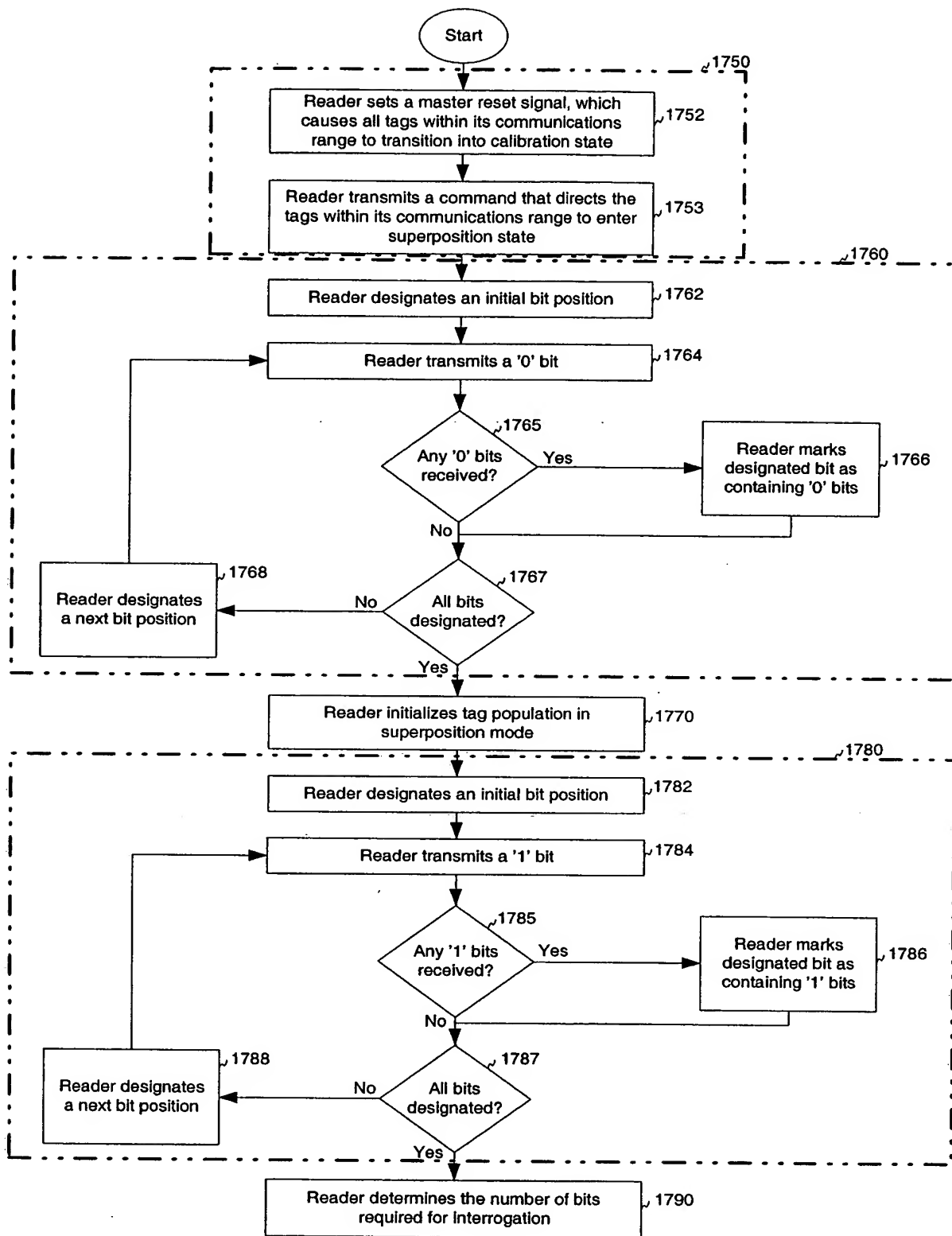


FIG. 17B

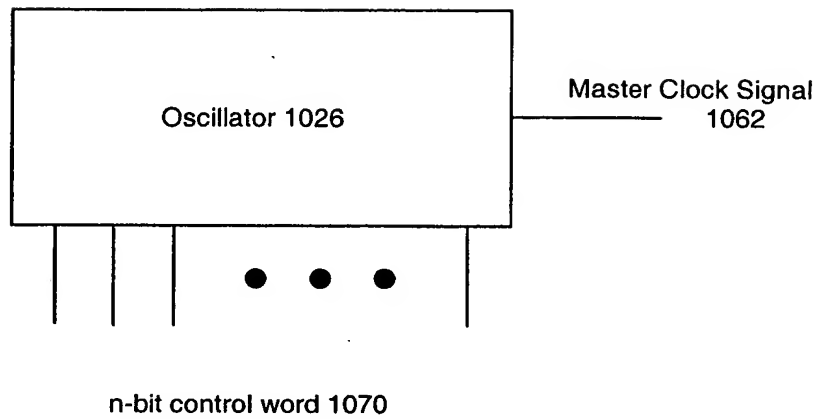


FIG. 18

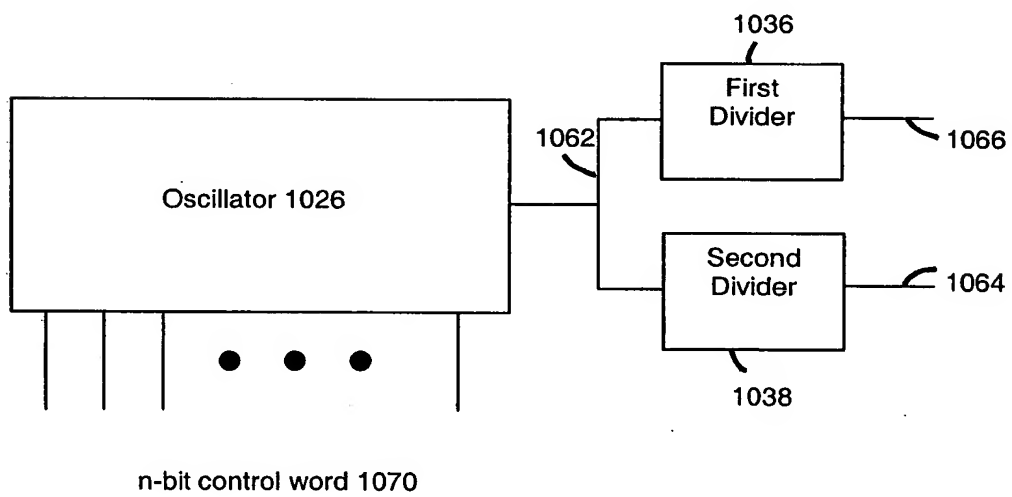


FIG. 19

10073000-00400

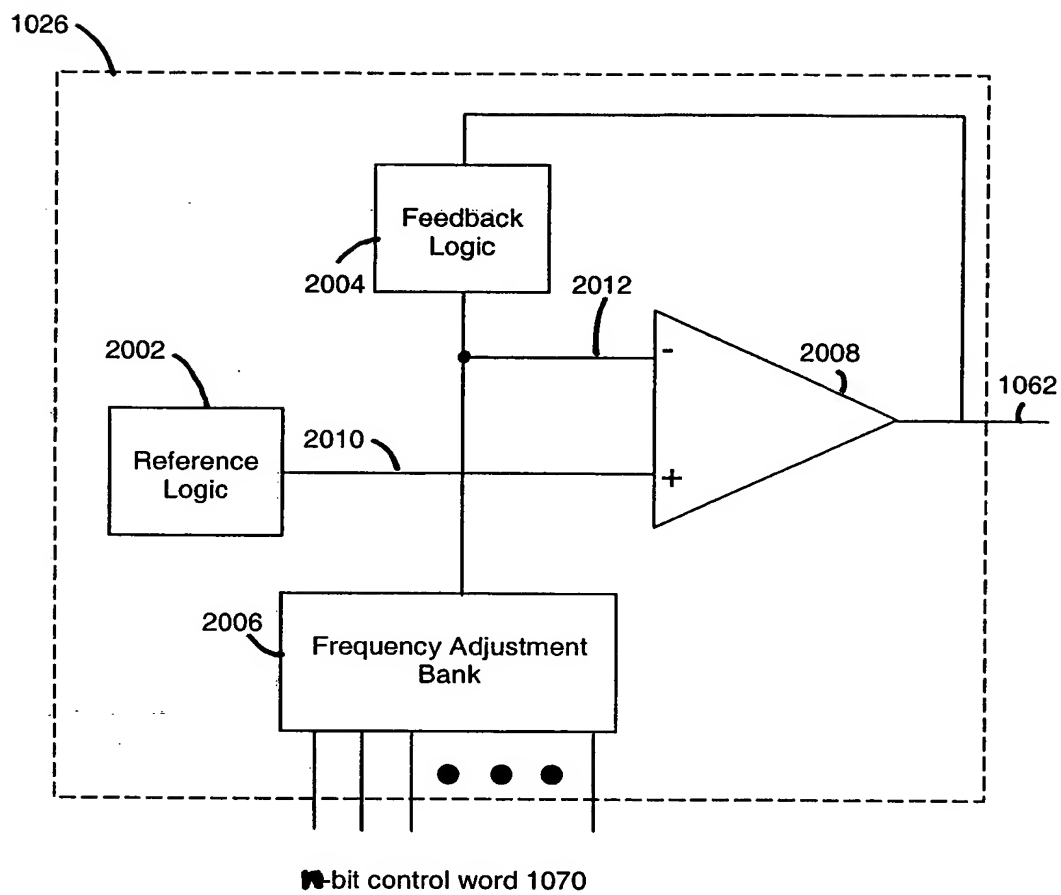


FIG. 20

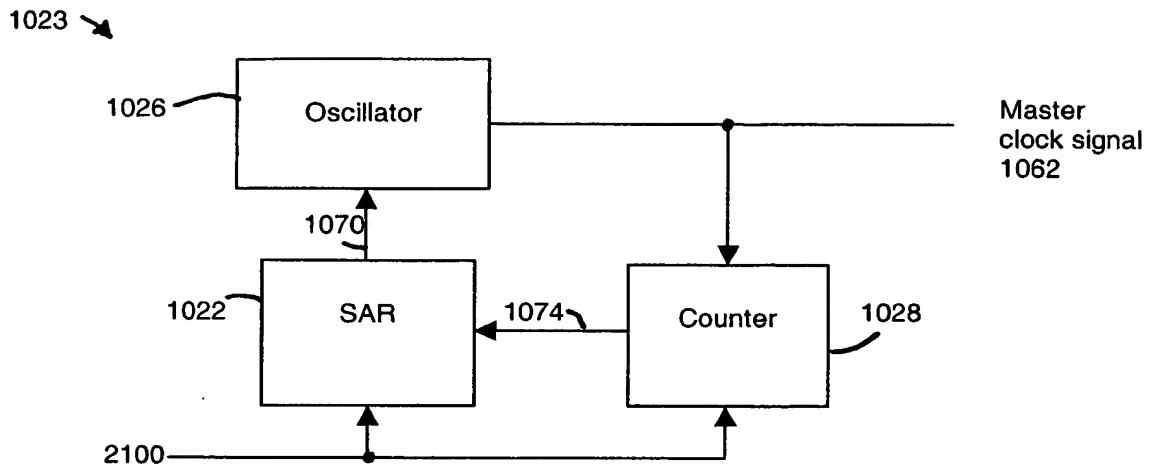


FIG. 21A

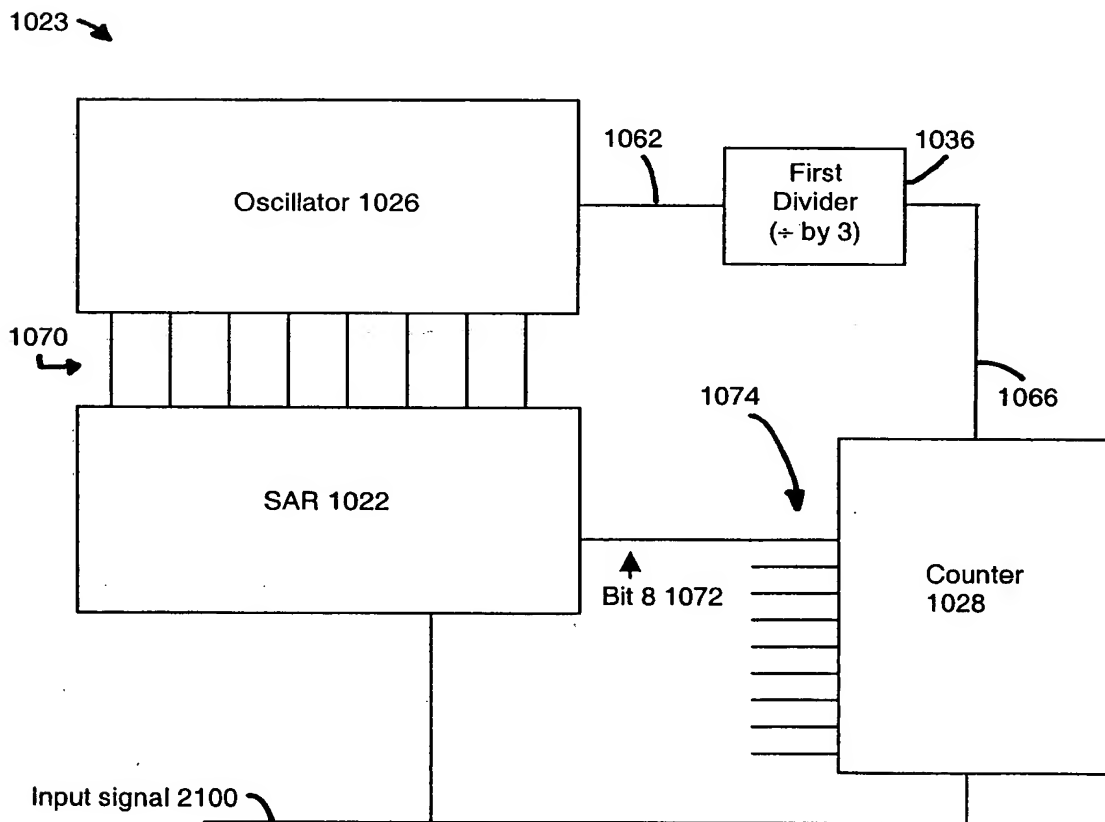


FIG. 21B

# Conceptual Implementation of SAR calibration

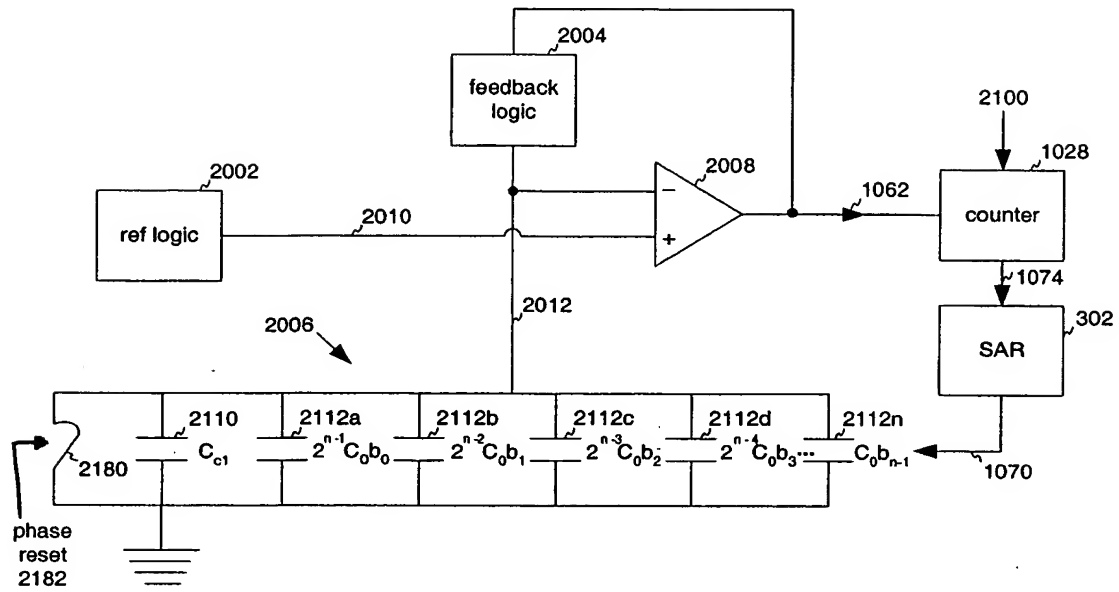


FIG. 21C

# Physical implementation of adjustable capacitor bank

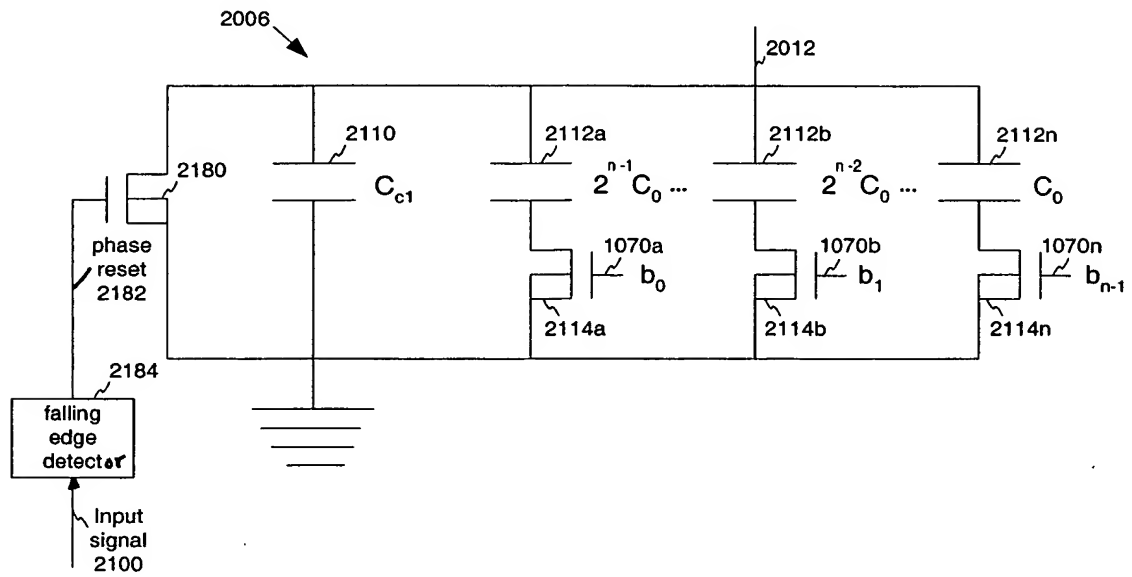
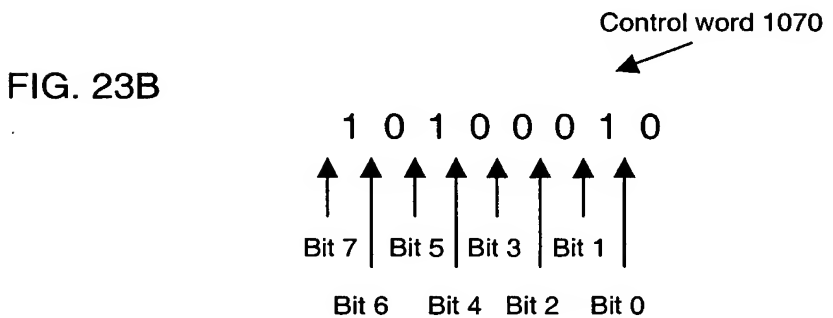
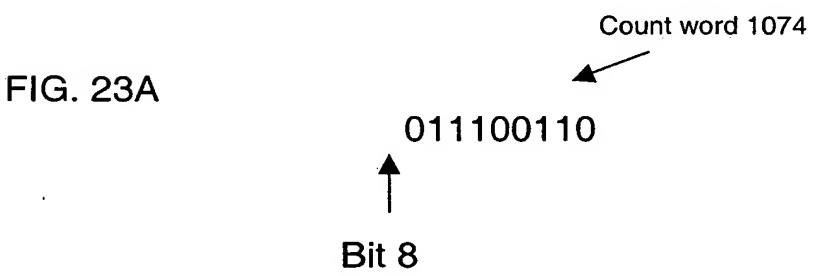
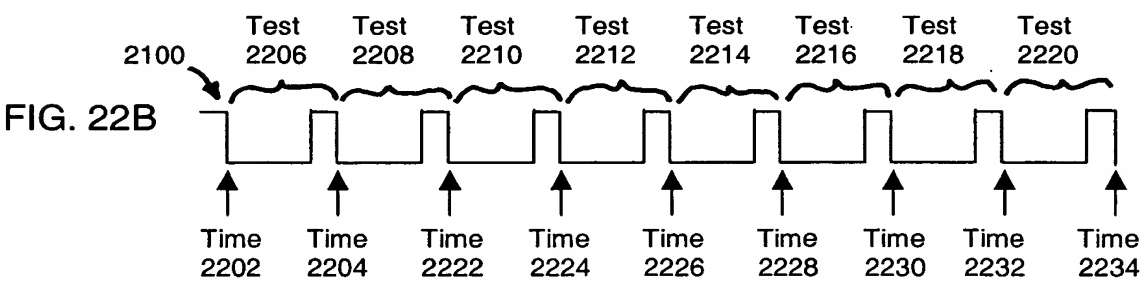
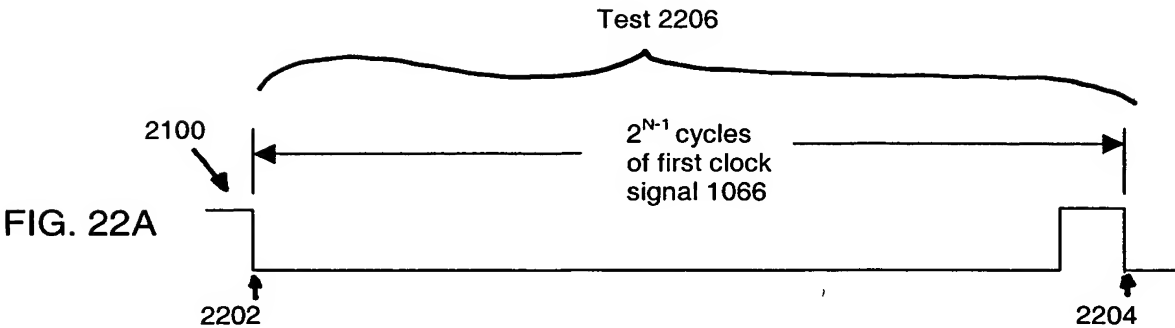


FIG. 21D

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2025-03-07 10:20:00

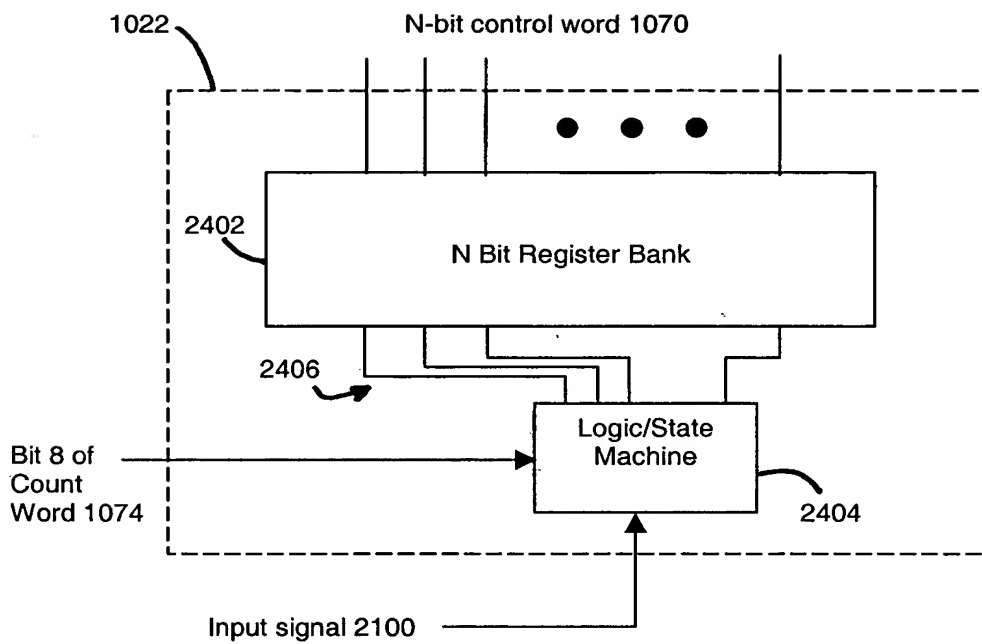
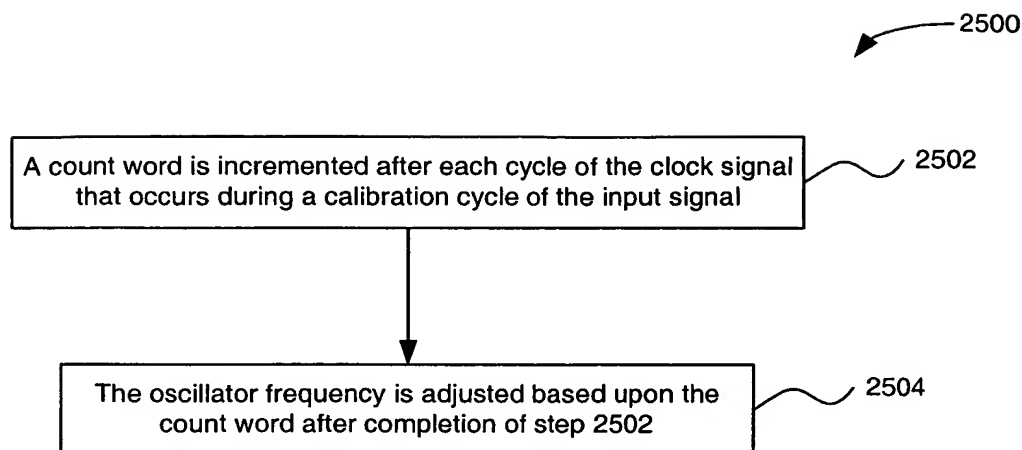
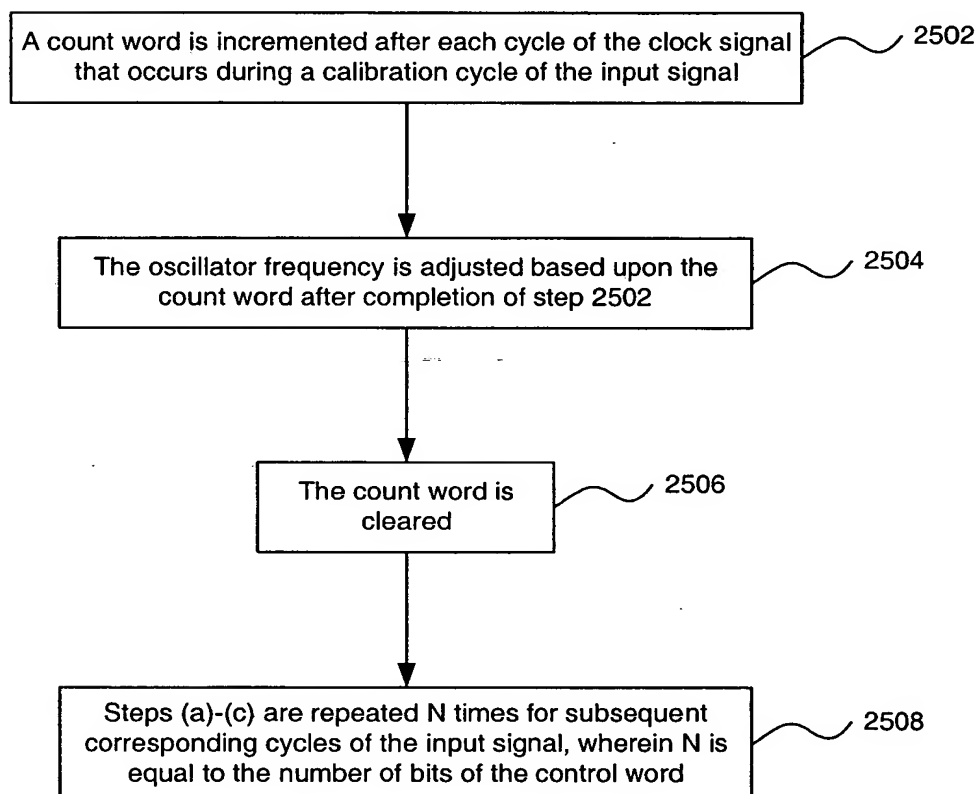


FIG. 24



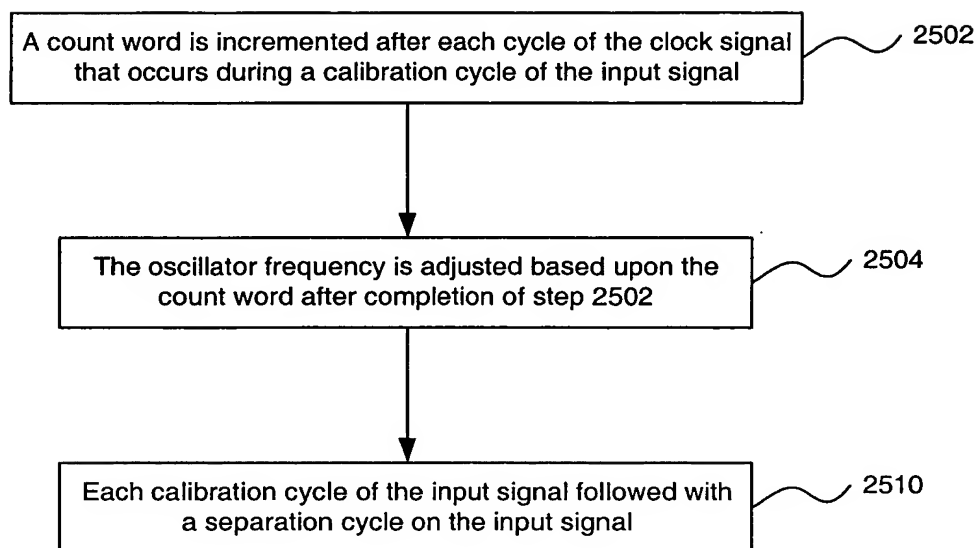


**FIG. 25A**



**FIG. 25B**

2024-03-08 10:07:30



**FIG. 25C**

2025-08-08 10:07:30

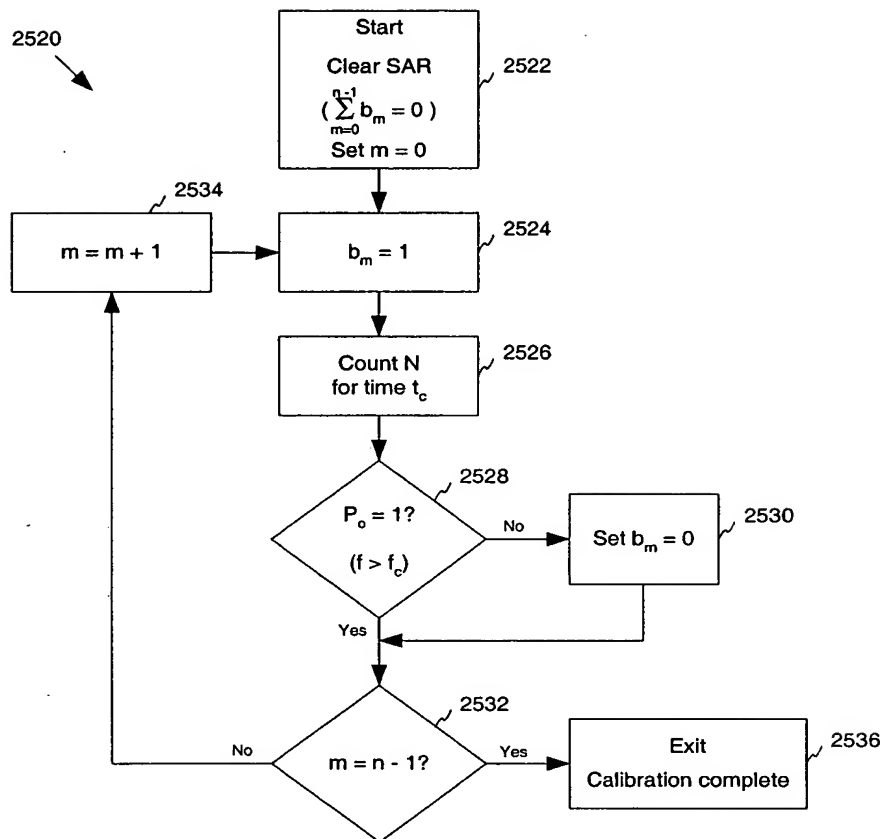


FIG. 25D

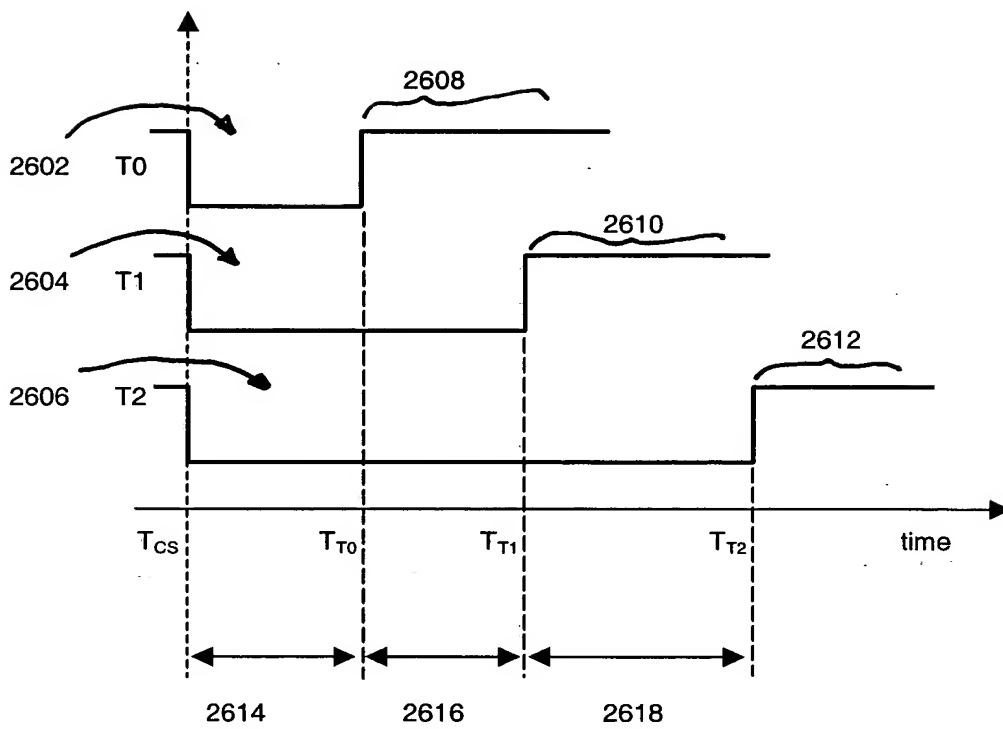


FIG. 26A

2021-20b.vsd/29

Data Symbol Timing Chart

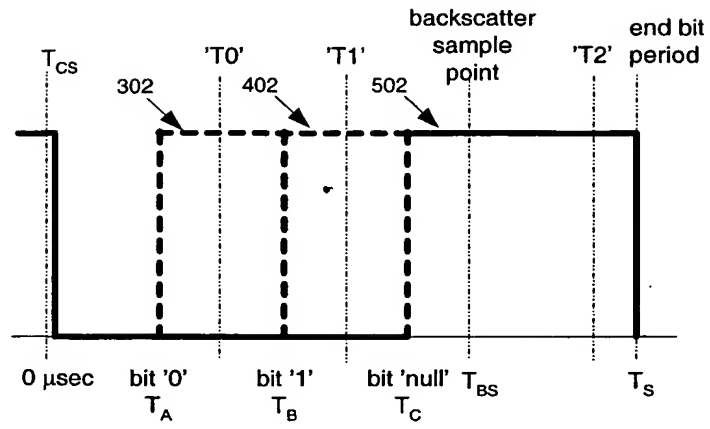


FIG. 26B

2021-20b.vsd/30

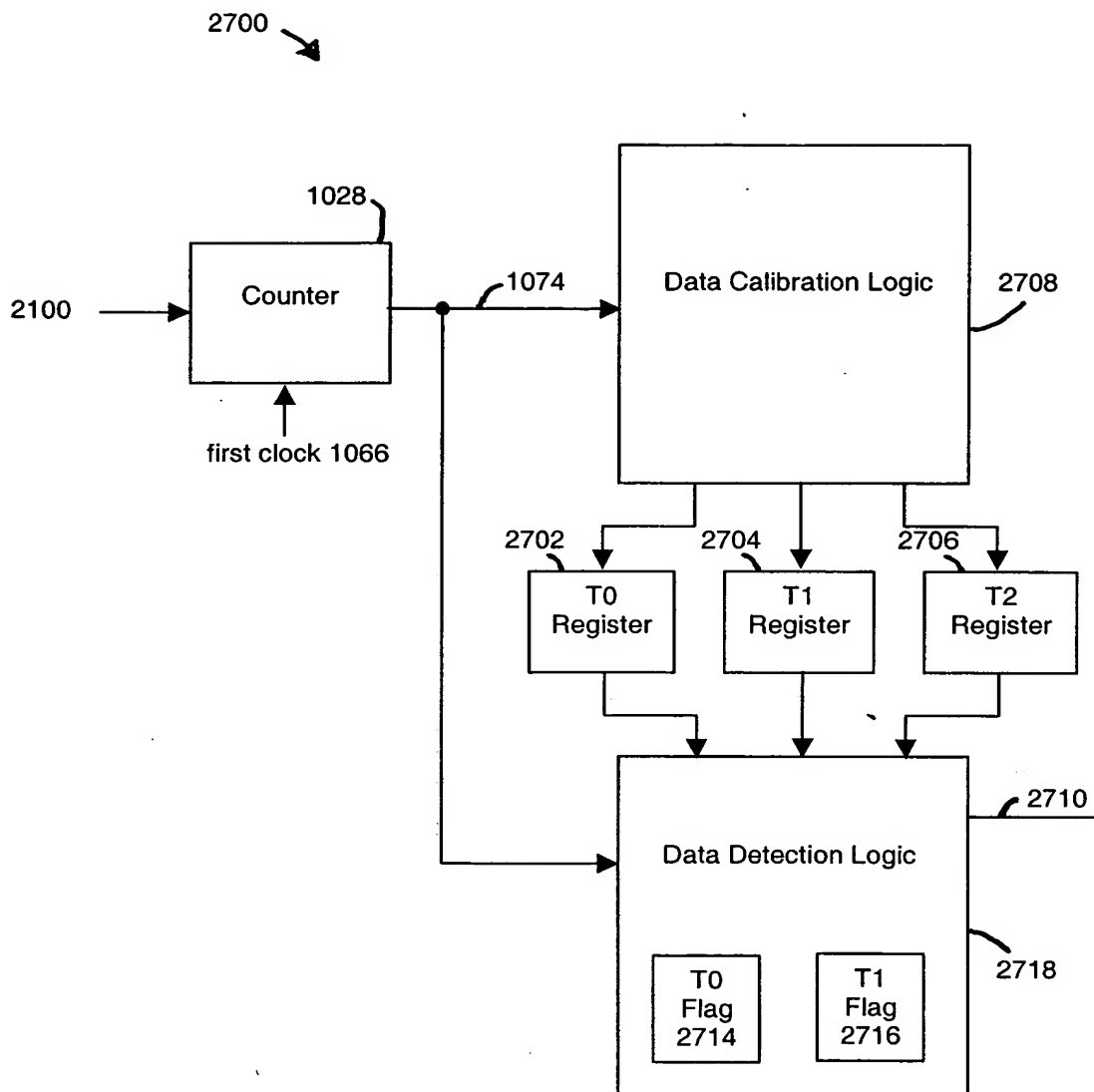
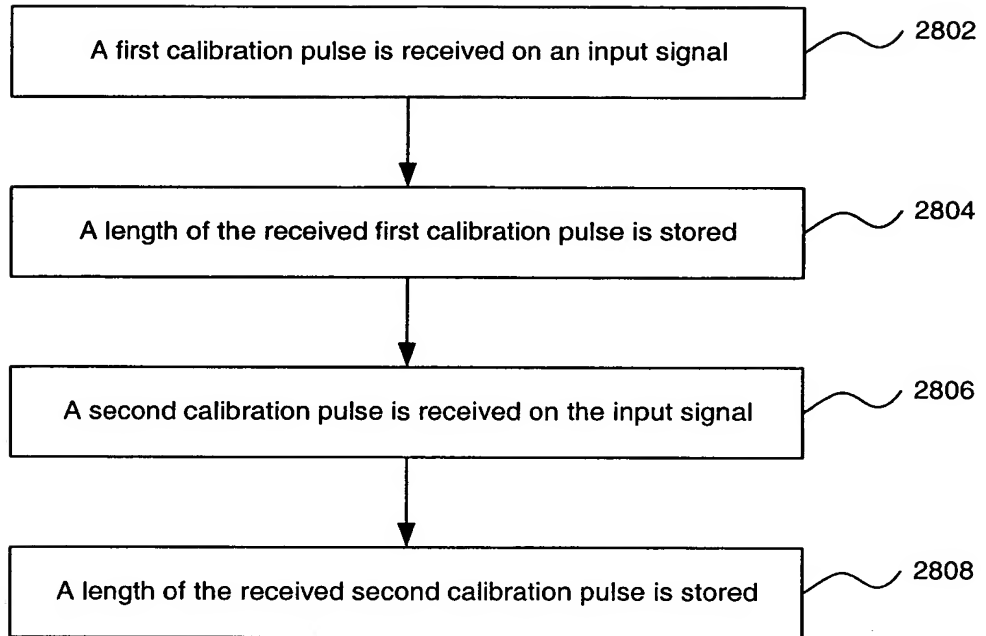


FIG. 27

2800



**FIG. 28A**

2800

From flowchart 2800

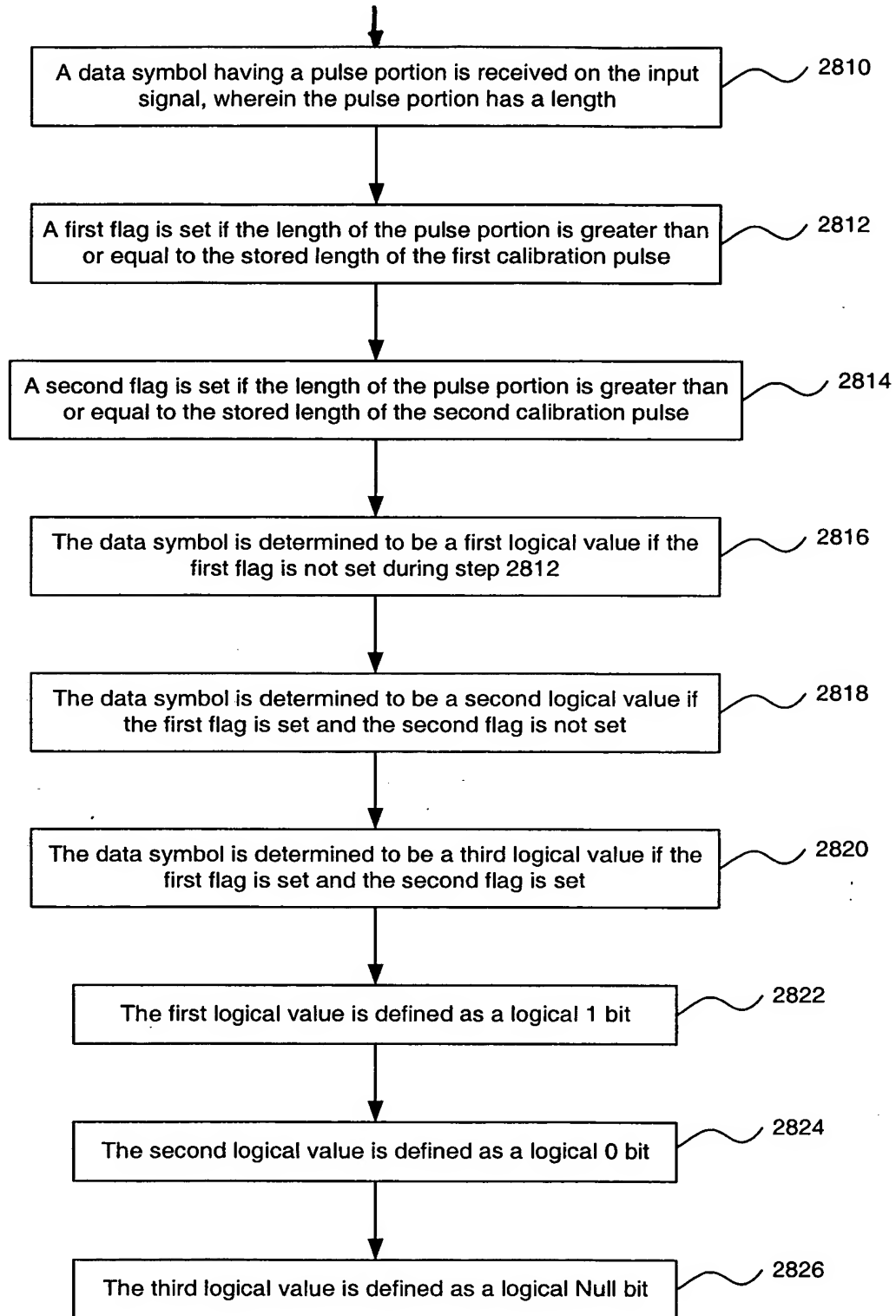
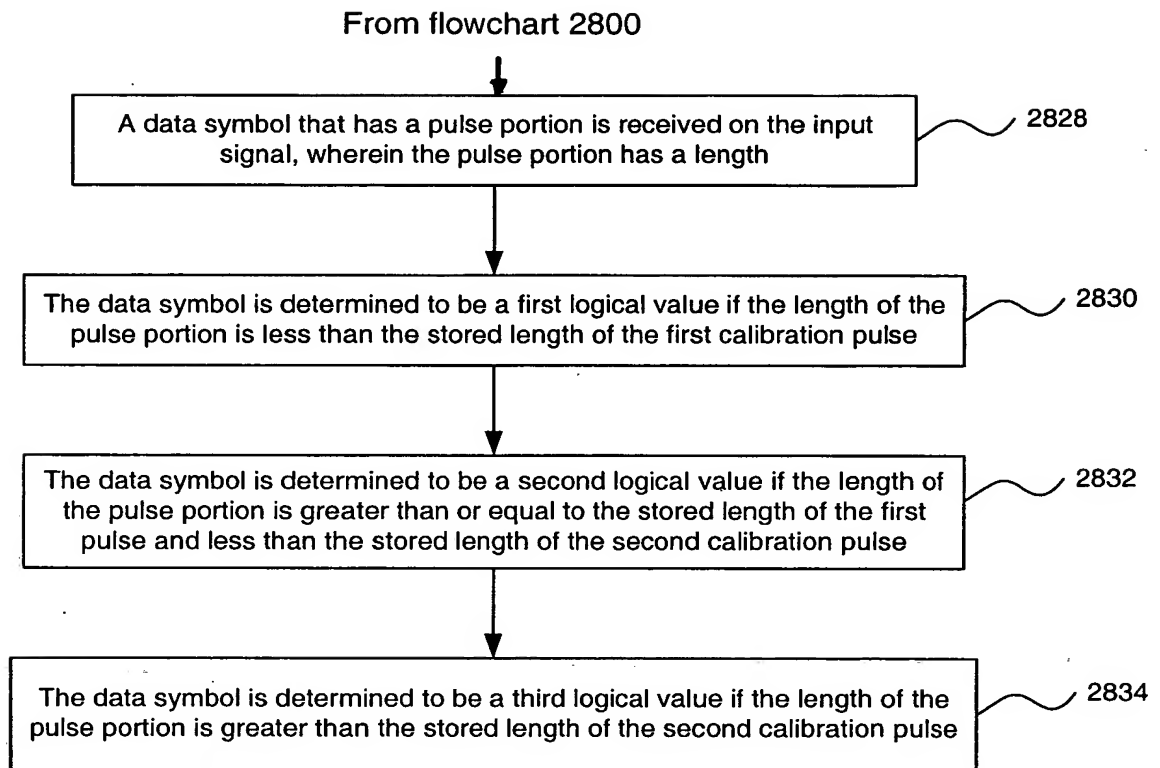


FIG. 28B

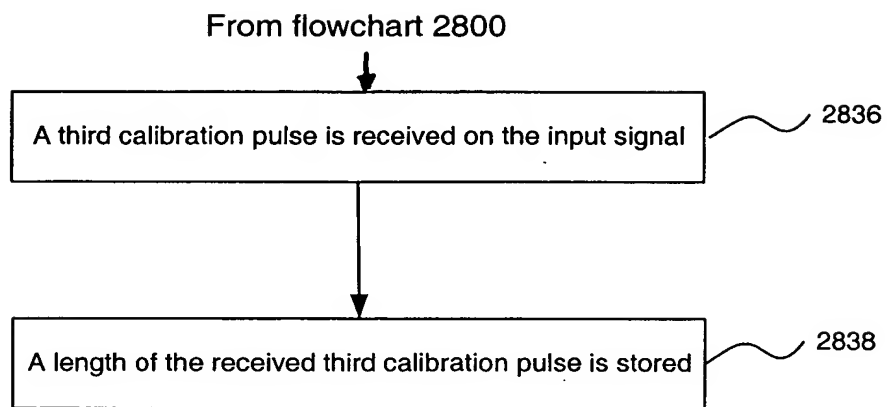


10073000-00400



**FIG. 28C**

2023-08-08 10:23:00



**FIG. 28D**

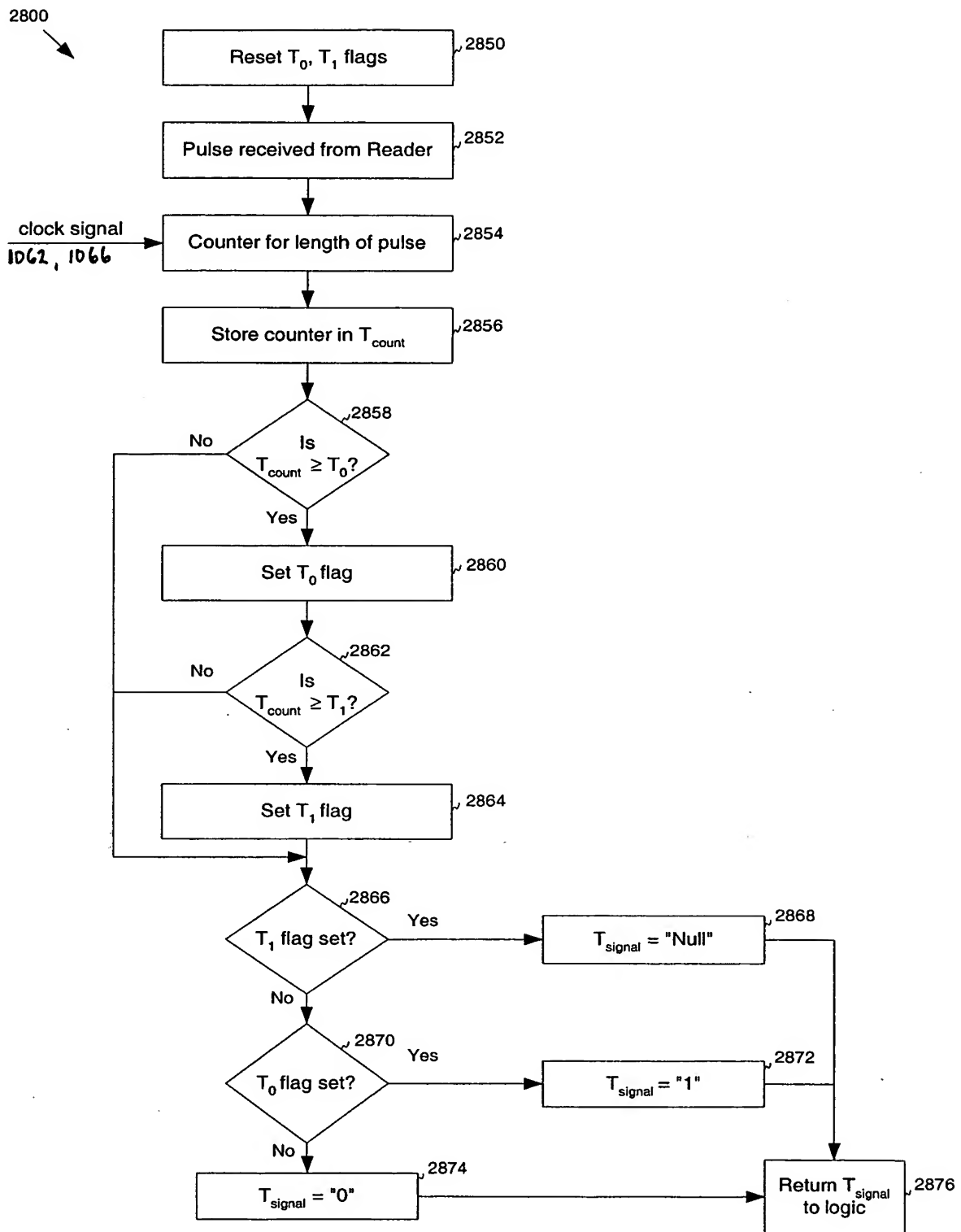


FIG. 28E

2025-03-29 09:02:00

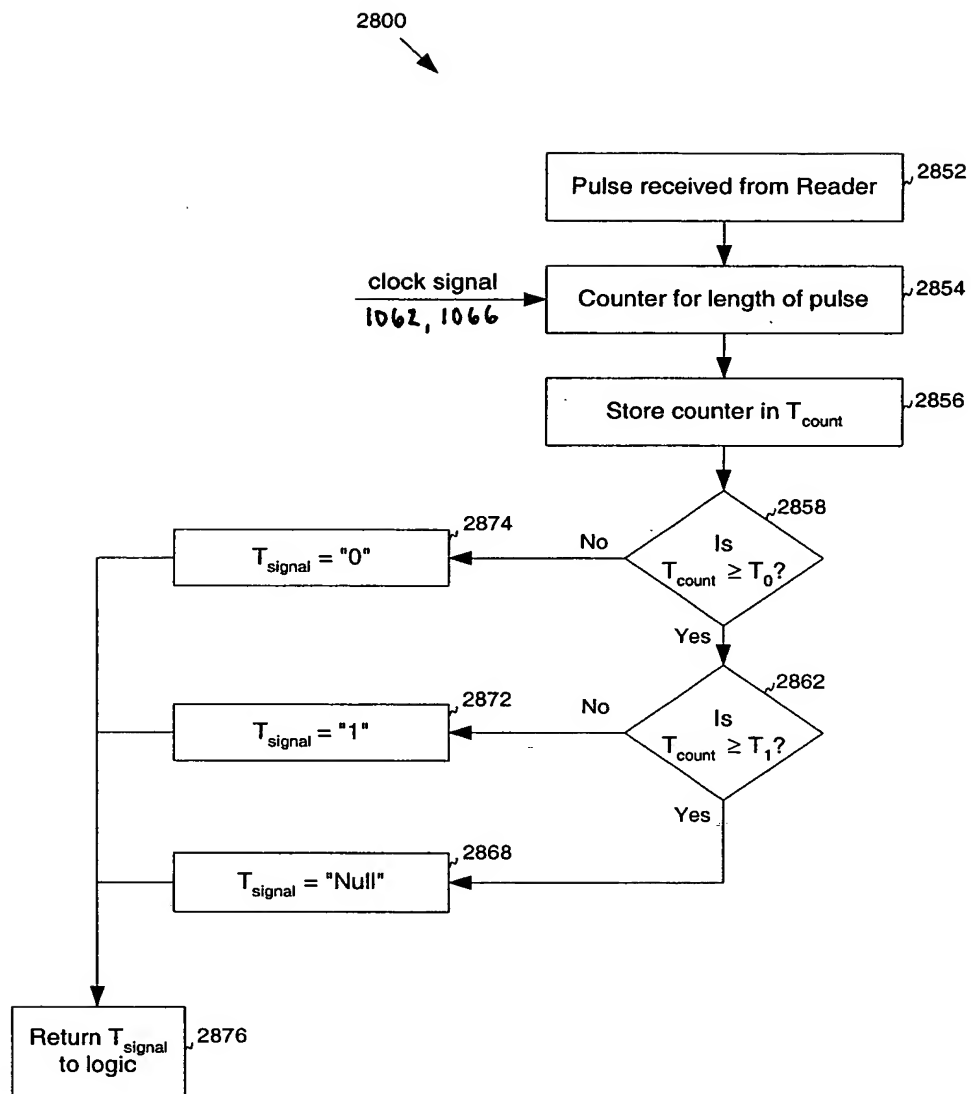
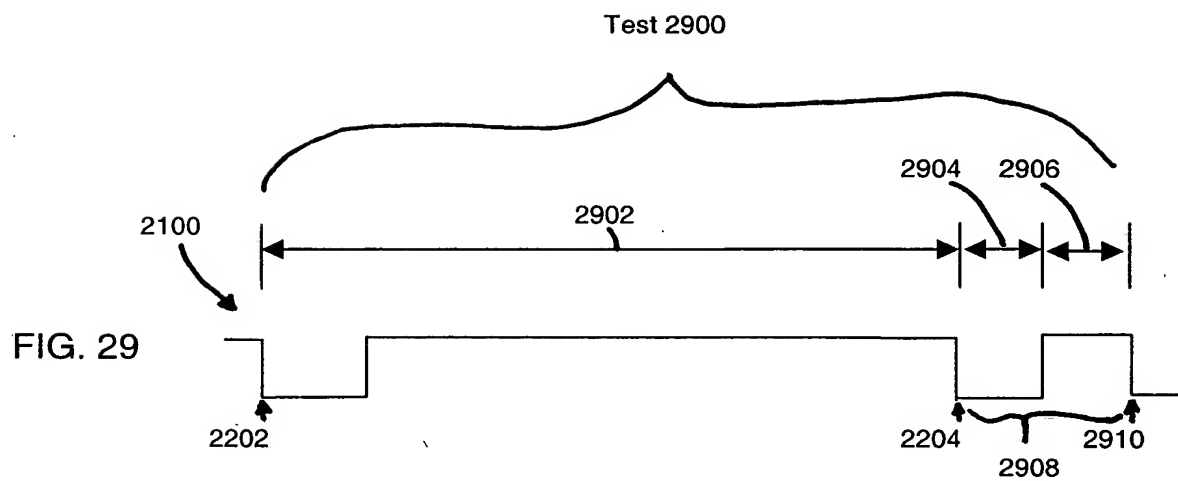
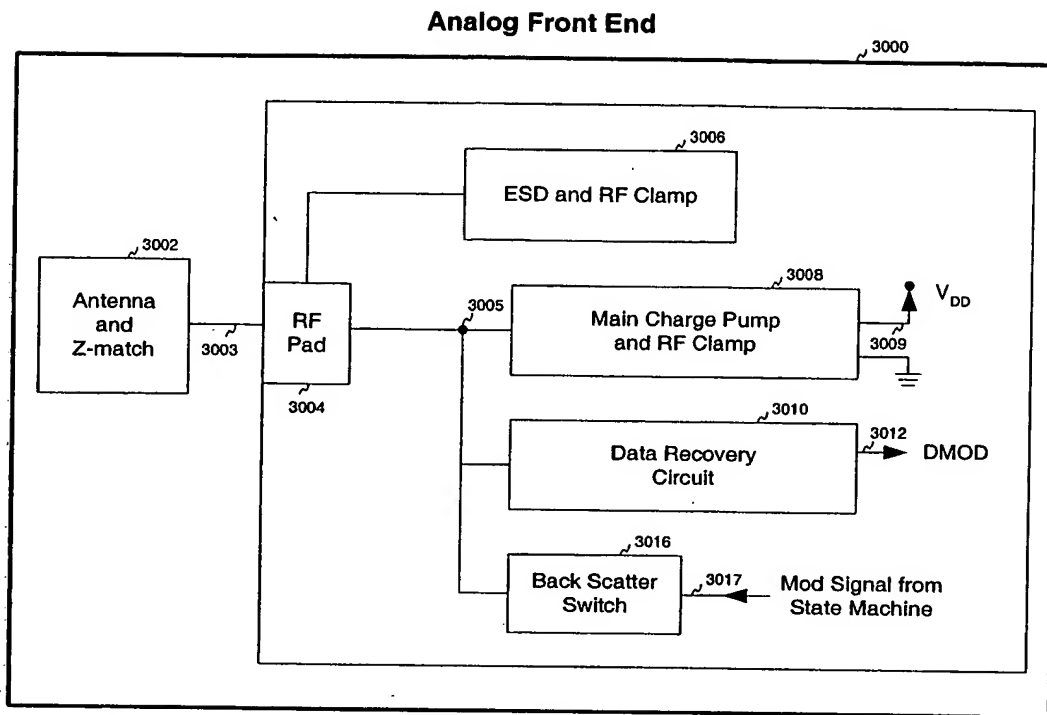


FIG. 28F

10073000-021202



20073006-021207



**FIG. 30**



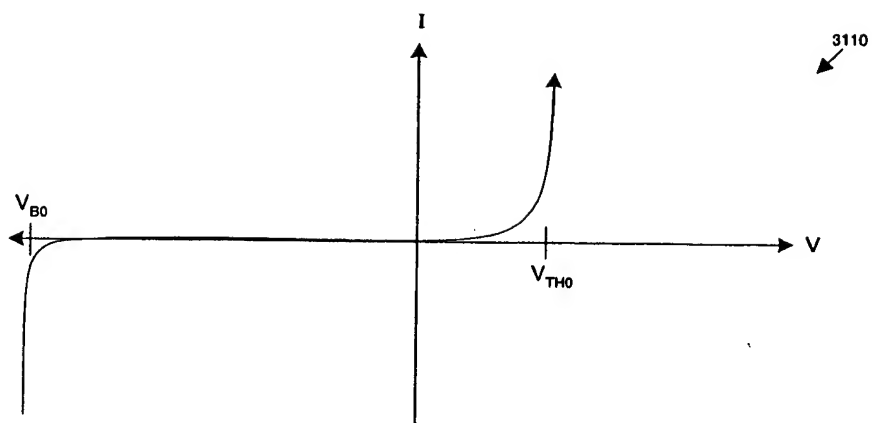
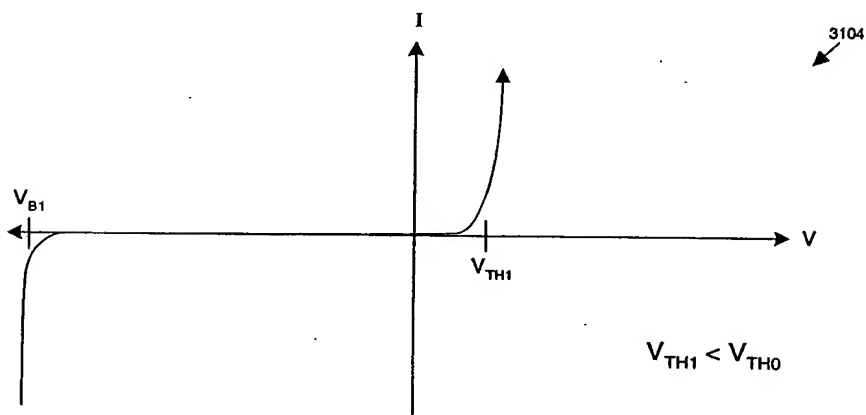
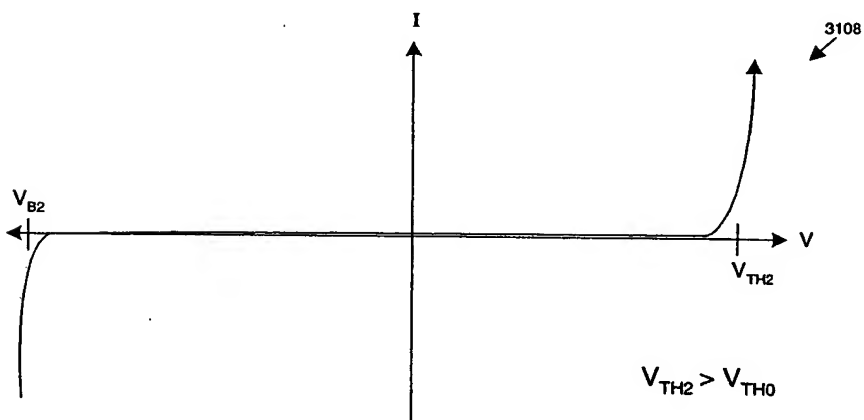


FIG. 32A



$$V_{TH1} < V_{TH0}$$

FIG. 32B

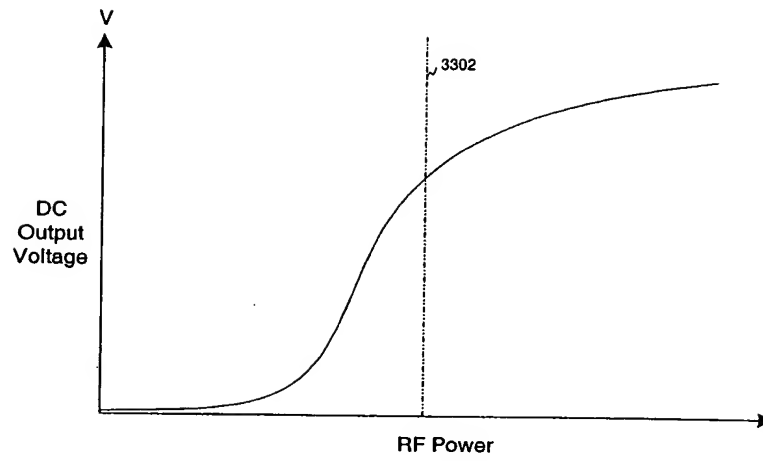


$$V_{TH2} > V_{TH0}$$

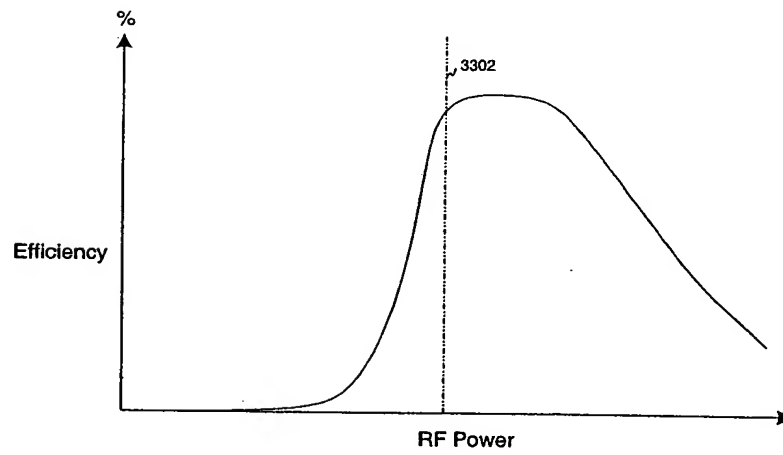
FIG. 32C



10073000-021203



**FIG. 33A**



**FIG 33B**

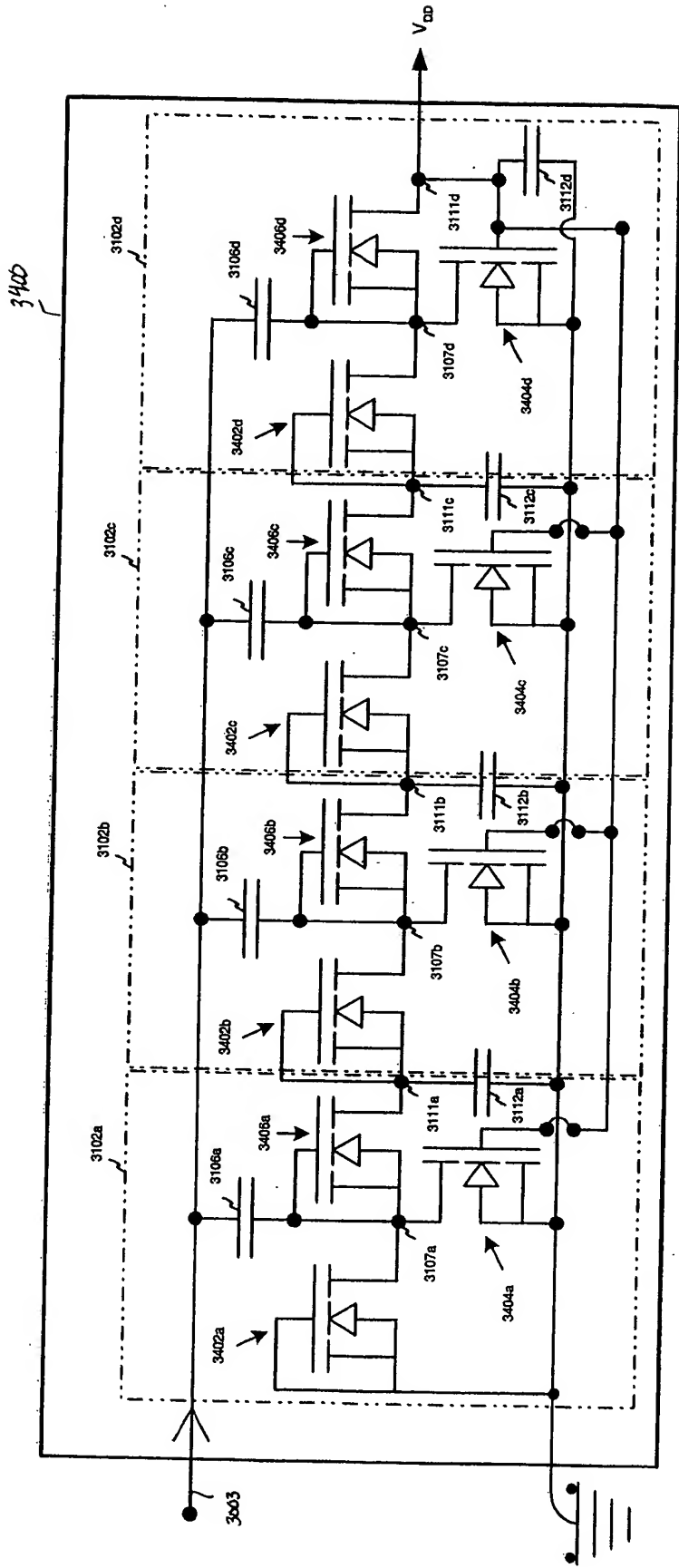


FIG. 34A

3400

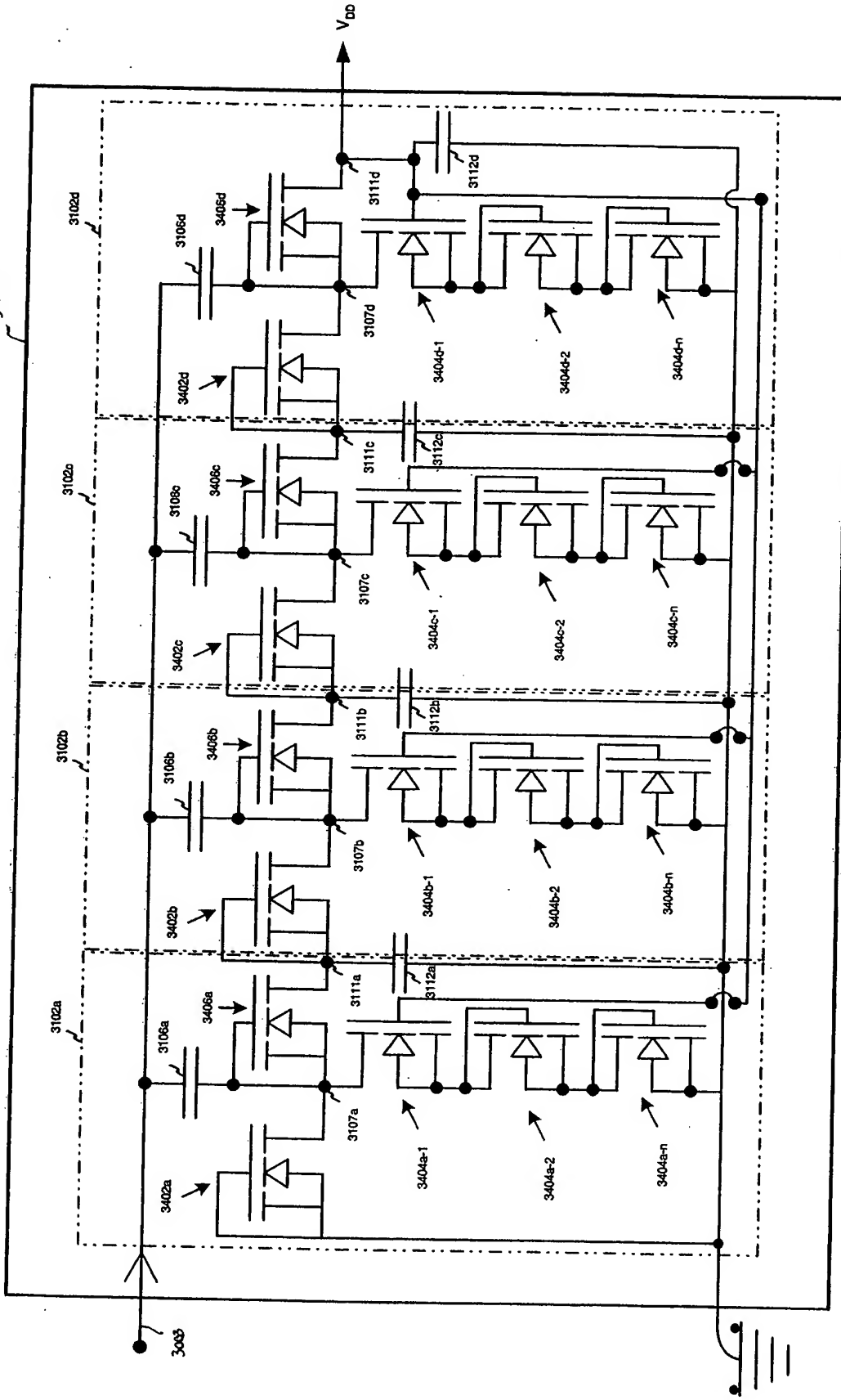


FIG. 34B

2025-08-22 10:00:00

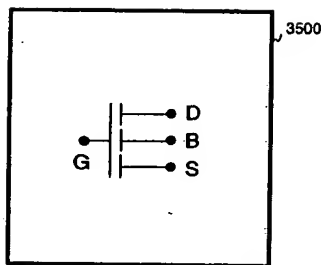


FIG. 35A

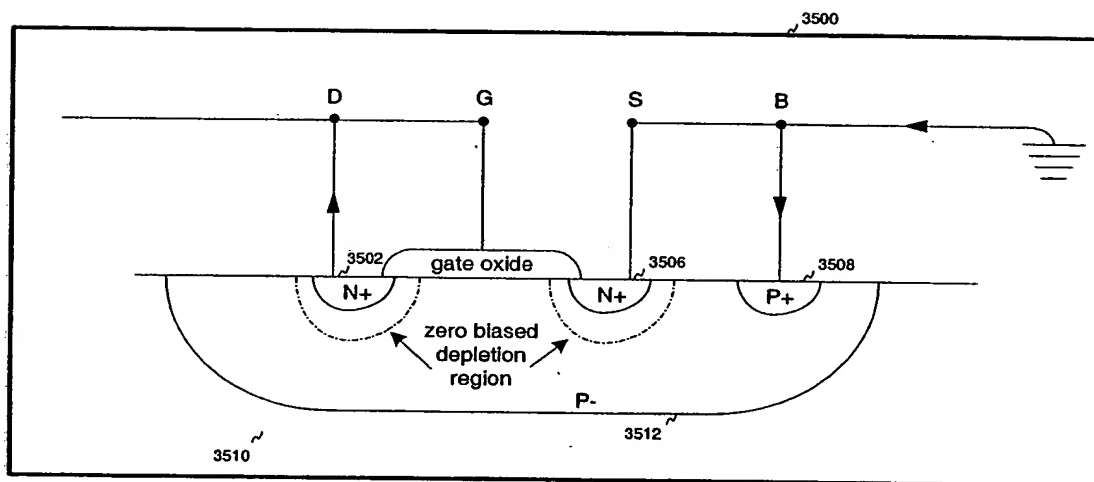
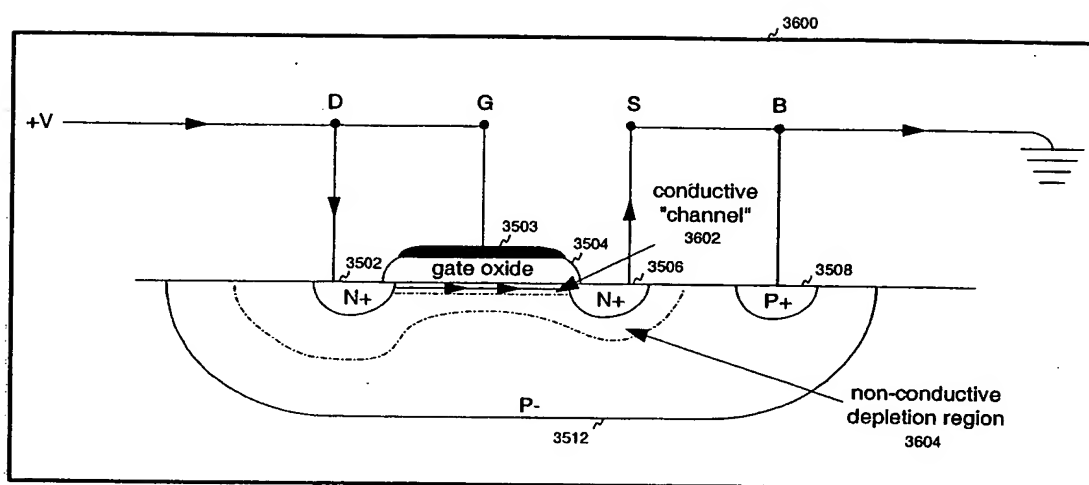
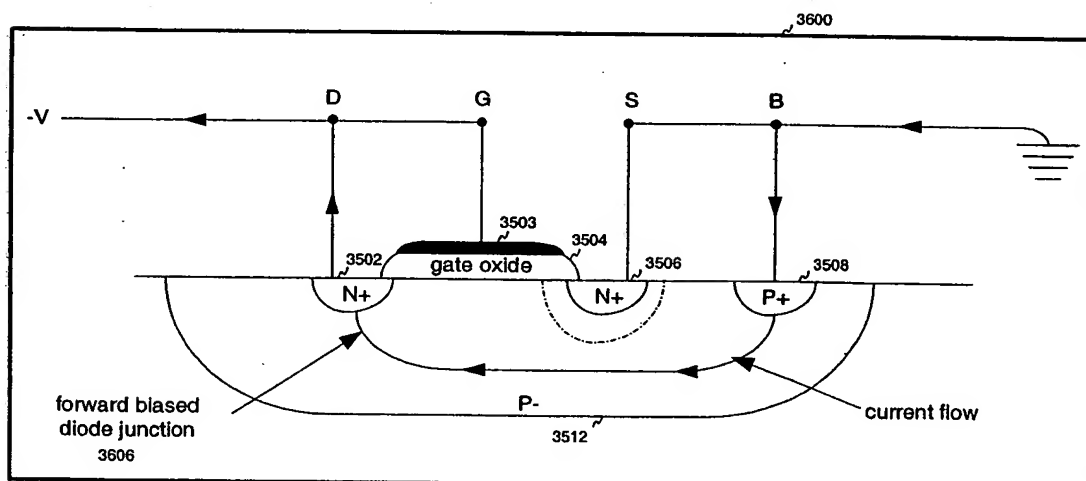


FIG. 35B

**FIG. 36A**



**FIG. 36B**



**FIG. 36C**

2025-08-20 00:00:00

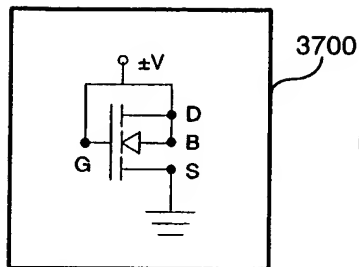


FIG. 37A

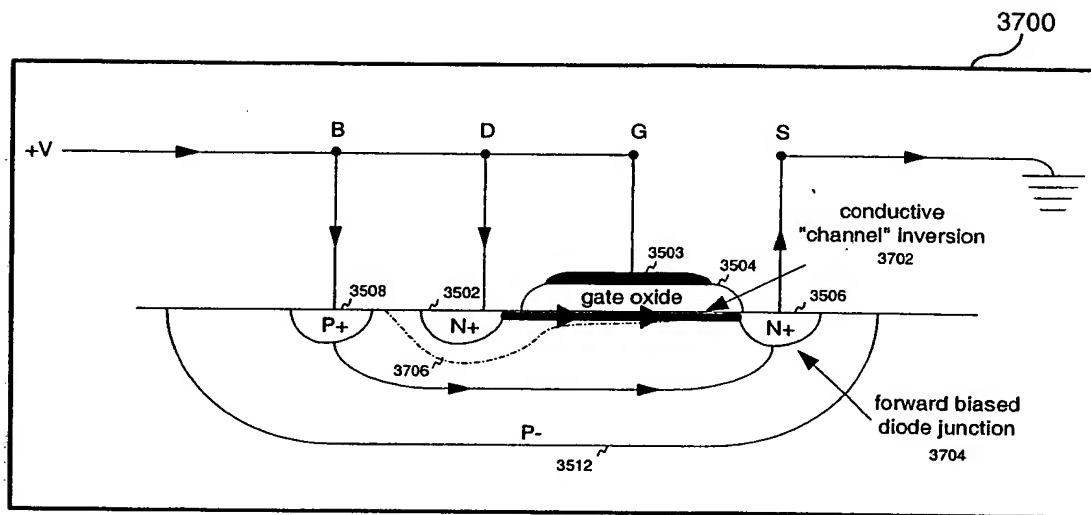


FIG. 37B

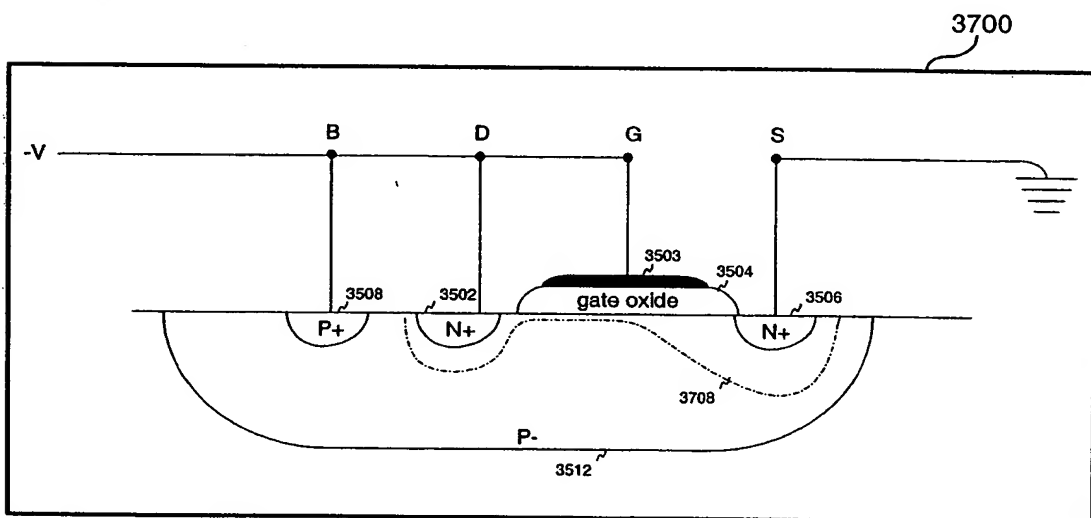
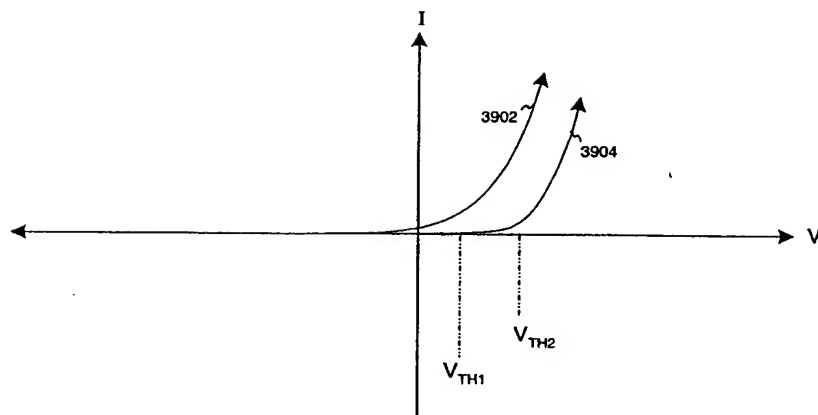


FIG. 37C

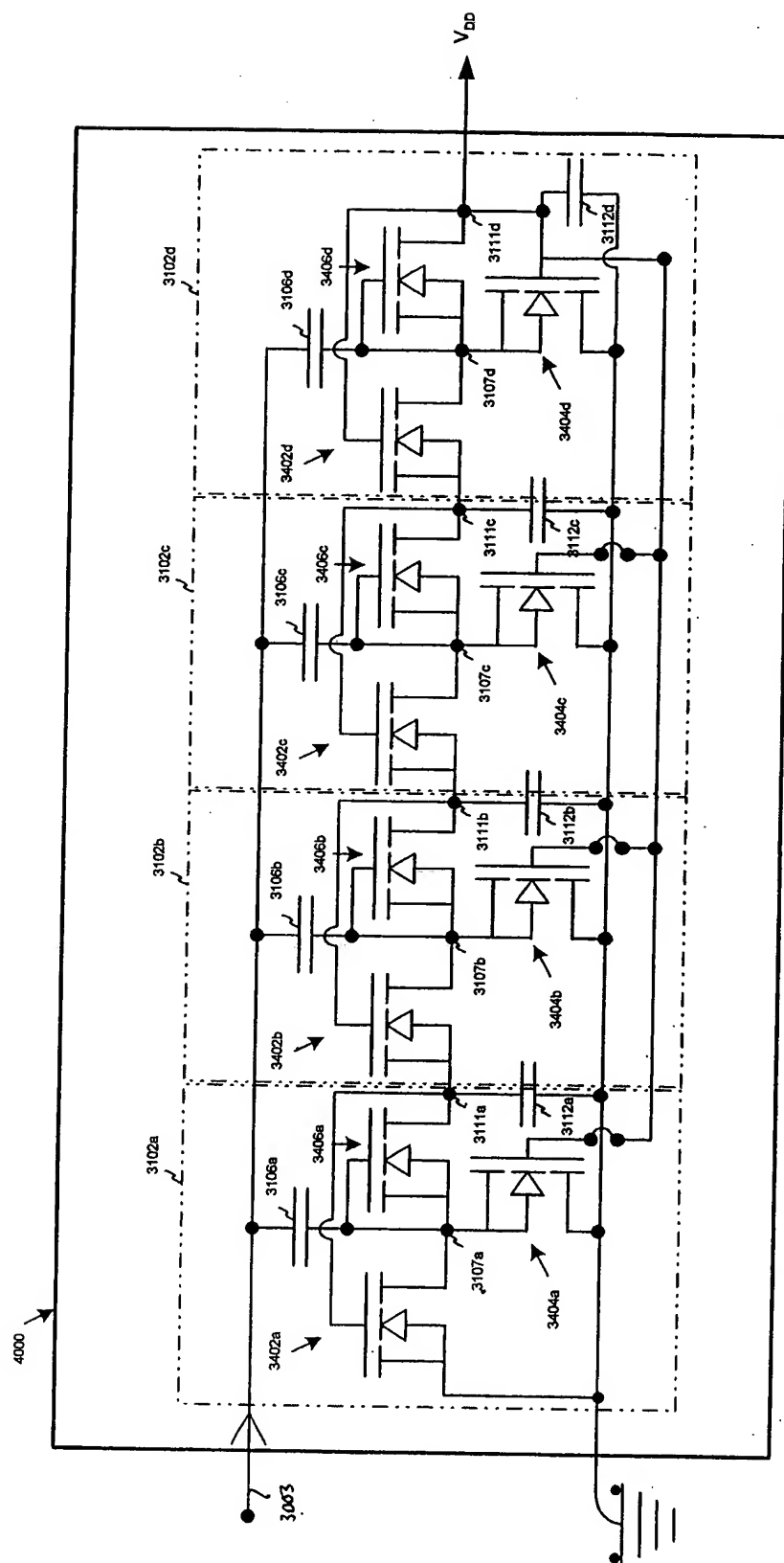


10073000-004200



**FIG. 39**





**FIG. 40A**

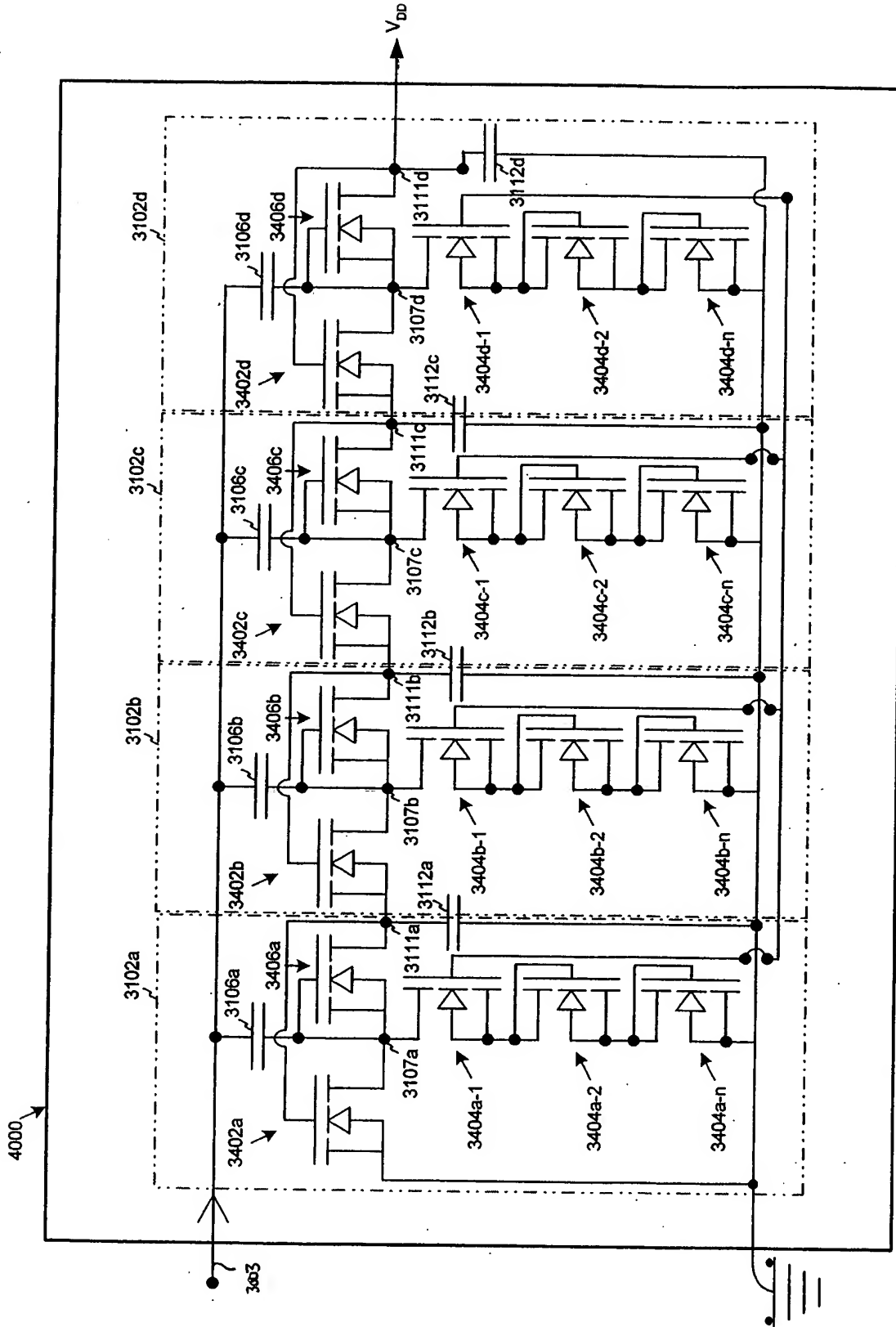


FIG. 40B

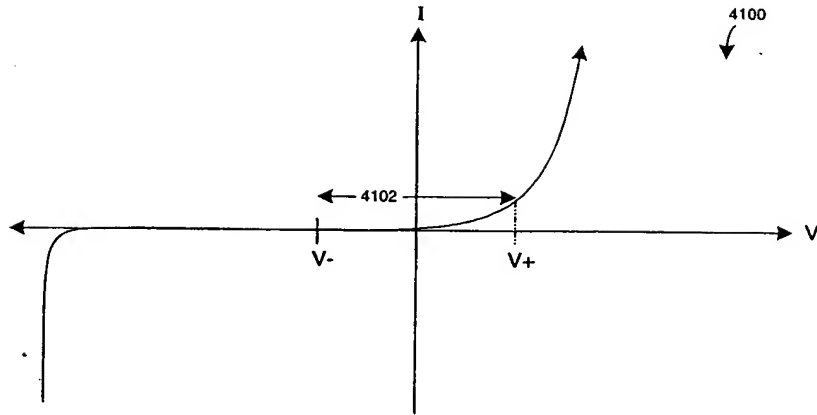


FIG. 41A

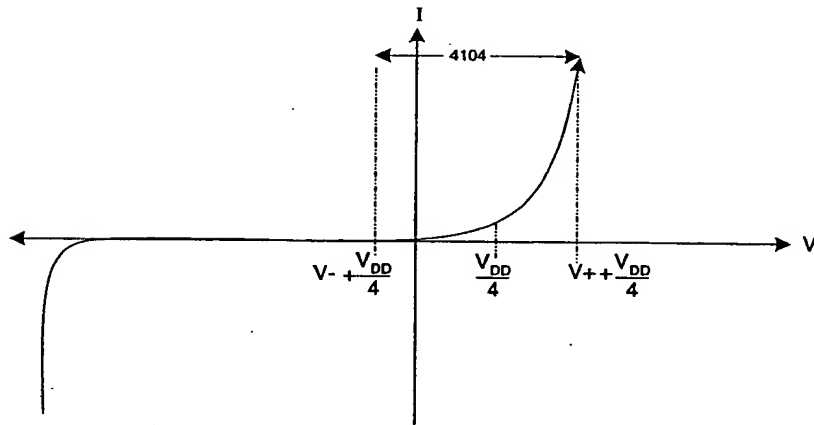


FIG. 41B

2025-03-07 10:00:00

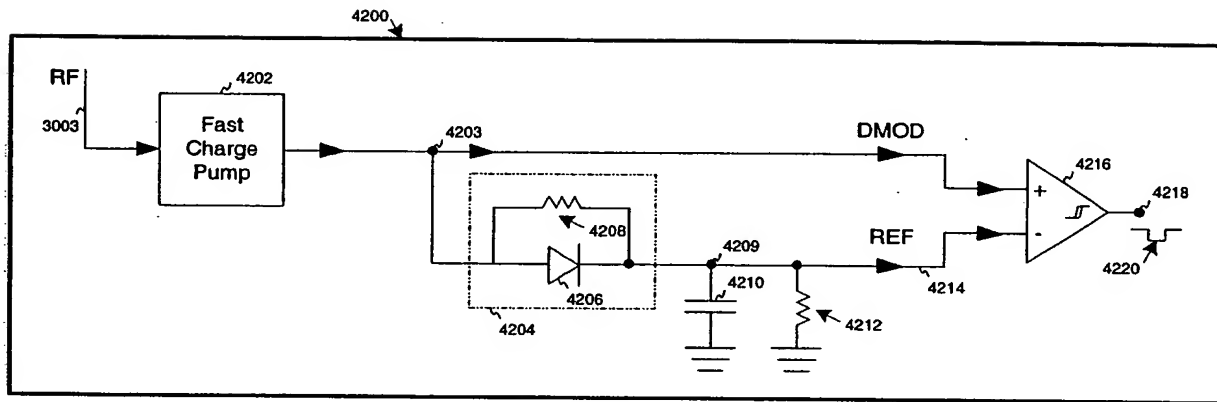
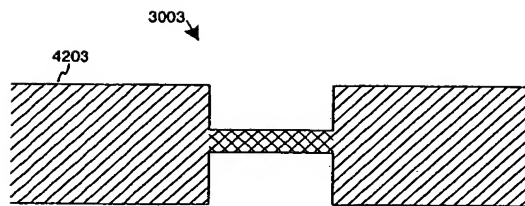
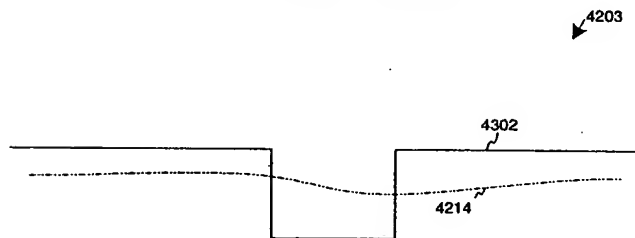


FIG. 42

2025-08-20 10:00:00



**FIG. 43A**



**FIG. 43B**

2025-08-08 00:00:00

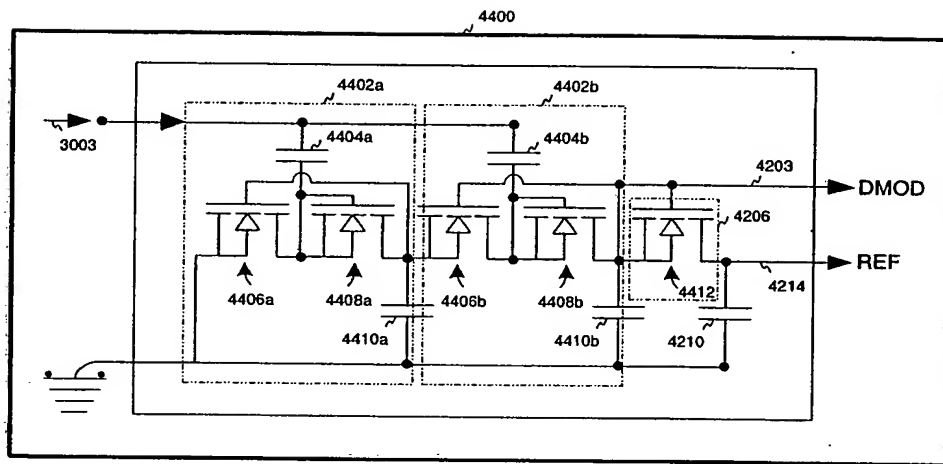


FIG. 44

2025-08-08 10:07:30

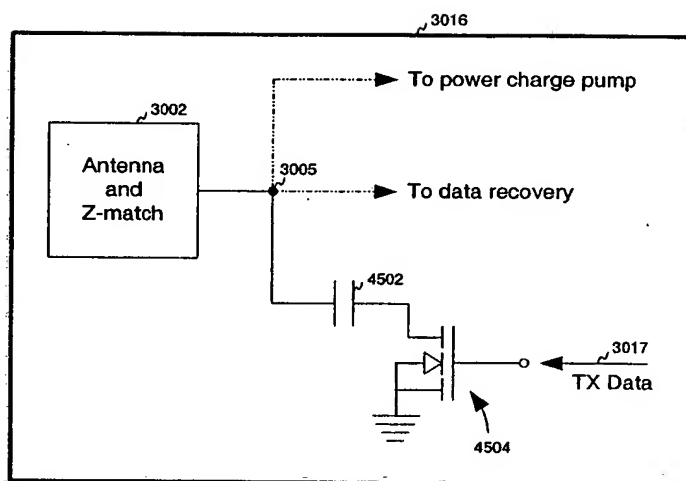


FIG. 45